PUBLICATION NO. 980499

5100 AF DIGITAL MULTIMETER

ME-503/U

RACAL-DANA

RACAL-DANA INSTRUMENTS INC.
18912 Von Karman Ave., Irvine, CA 92715
Telephone: 714/833-1234, TWX: 910-595-1136, TLX: 67-8341

RACAL-DANA INSTRUMENTS LTD.
Duke Street, Windsor, Berkshire SL4 1SB, United Kingdom
Telephone: Windsor (07535) 69811, TLX: 847013

RACAL-DANA INSTRUMENTS S.A.
18 Avenue Dutartre, 78150 Le Chesnay, France
Telephone: (3) 955-8888, TLX: 697 215

RACAL-DANA INSTRUMENTS, LTD., DEUTSCHLAND
Hermannstrasse 29, D-6078 Neu Isenburg, Federal Republic of Germany
Telephone: 06102-2861/2, TLX: 412896

RACAL

PUBLICATION DATE: NOVEMBER 1978

PROPRIETARY NOTICE

This document and the technical data herein disclosed, are proprietary to Dana Laboratories, Inc., and shall not, without express written permission of Dana Laboratories, Inc., be used, in whole or in part to solicit quotations from a competitive source or used for manufacture by anyone other than Dana Laboratories, Inc. The information herein has been developed at private expense, and may only be used for operation and maintenance reference purposes or for purposes of engineering evaluation and incorporation into technical specifications and other documents which specify procurement of products from Dana Laboratories, Inc.

FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltages hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC Mains through an autotransformer (such as a Variac or equivalent) ensure that the instrument common connector is connected to the ground (earth) connection of the power mains.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adapter.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument.

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation section.
2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.
3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

TABLE OF CONTENTS

TABLE OF CONTENTS continued

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS continued

LIST OF TABLES

SECTION 1 GENERAL DESCRIPTION

1.1 INTRODUCTION.

1.1.1 The Model 5100AF Digital Multimeter (figure 1.1) is a five digit "Delayed Dual Slope" instrument with a sixth decade providing 100% overrange. Measurement capability is shown in table 1.1. The basic instrument is equipped for dc voltage measurements on five ranges, ac voltage measurements on four ranges and resistance measurements on six ranges. The basic instrument is also capable of measuring ratio of two DC voltages (3-wire connection). The instrument is equipped with an Averaging AC Converter.

1.1.2 Range can be selected manually or automatically (autorange). In Autorange the proper range for a particular measurement is selected automatically (full scale is defined as "100 000" on any range). The instrument "upranges" at 200,000 counts and "downranges" at 10,000 counts. Polarity selection is also automatic and is displayed on the front panel.

Table 1.1 - Measurement Capability

Range	Function			
	DCV	Ohms	DC Ratio X10	ACV
.1V	■		.01:1	
1V	■		.1:1	■
10V	■		1:1	■
200V	■		10:1	■
1000V	■		100:1	■
.1 KΩ		■		
1 KΩ		■		
10 KΩ		■		
200 KΩ		■		
1 MΩ		■		
10 MΩ		■		

1.2 ELECTRICAL DESCRIPTION.

1.2.1 The Dana Model 5100AF Digital Multimeter consists of three parts: the Signal Conditioning section, the Digital section, and the Analog-to-Digital (A/D) converter.

1.2.2 The signal conditioning section modifies the input signal before reaching the A/D converter. For dc measurement, the input signal is scaled, if required, to a 2 volt (200,000 count) signal and filtered if required. For ac or resistance measurement, the input signal is scaled, if necessary, and converted to a proportional dc value. The dc value is filtered, if necessary, and routed to the A/D converter.

1.2.3 The A/D converter changes a dc signal fed into it into a representative digital signal. The method used to perform this task is called Delayed Dual Slope integration.

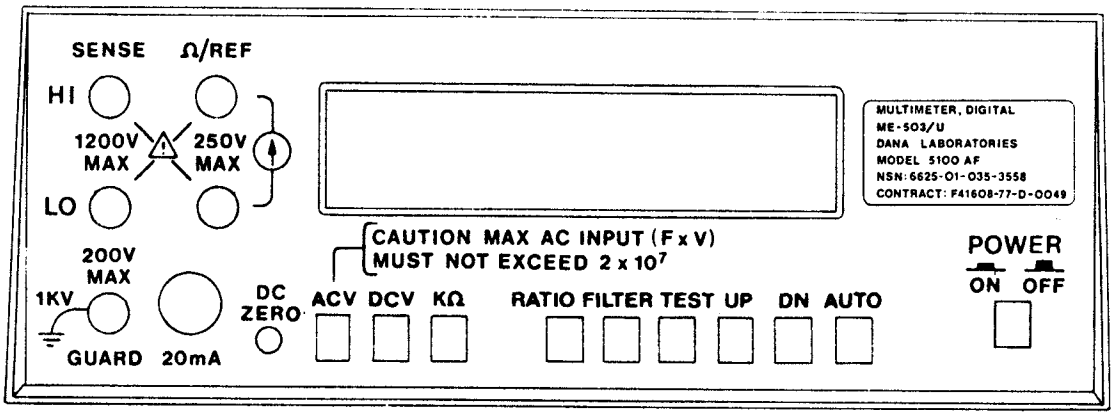


Figure 1.1 - Model 5100AF

1.2.4 The digital section measures the output of the A/D converter to produce a numeric value on the instrument display that represents the value of the input signal. The digital section also provides range control and decimal placement.

1.3 SPECIFICATIONS.

1.3.1 Specifications are provided in table 1.2.

Table 1.2 - Specifications

GENERAL	
Maximum Counts:	200,000 (full scale + 100% overrange)
Display:	5 full decades plus overrange digit (.43 inch (1.1 cm) high LEDs), polarity annunciator and automatic decimal point
Read Rate:	5 readings per second
Ranging:	Manual and automatic. Up ranges automatically at 200,000 counts and down ranges at 10,000 counts
Overrange Indication:	"200000" flashing on display
Maximum Common Mode Voltage:	1000V between guard and earth ground 200V between "–" input and guard
Power Requirement:	115 and 230V ± 10%; 50 – 400 Hz; 18 watts maximum
Weight:	3 Kg (6.6 lbs.)
Dimensions:	Height x Width x Depth 73 x 200 x 250 mm 2.87 x 7.87 x 9.84 inches
Warm up Time:	30 minutes to full accuracy
Operating Temperature:	0°C to +55°C
Storage Temperature:	–40°C to +75°C
Warranty:	12 months – repair or replace malfunctions due to faulty workmanship or component failure

DC VOLTS (5 Ranges)	
Full Range Display:	±.100000, ±1.00000, ±10.0000, ±100.000, and ±1000.00
Resolution:	.001% of range on all ranges
Overrange:	100% on all ranges except 1000 range, 10% ±1100V DC maximum input
Accuracy: (25°C ± 2°C) to 50% R.H. for Short-Term Stability, 72 hrs.	.1 and 1 range ±0.006% of reading + (±0.005% of range) 10, 100, & 1000 range ±0.006% of reading + (±0.001% of range)
(20°C to 30°C) to 70% R.H. for Long-Term Stability, 6 mo.	All ranges ±0.01% of reading + (±0.005% of range)
(0°C to 40°C) to 100% R.H. for Long-Term Stability, 6 mo.	All ranges ±0.04% of reading + (±0.02% of range)
(40°C to 55°C) Relative Humidity to decrease linearily from 100% @ 40°C to 20% @ 55°C for Long-Term Stability, 6 mo.	All Ranges ±0.04% of reading + (±0.02% of range)
Input Resistance:	.1, 1, 10, & 100 ranges 100 MΩ 1000 range 10 MΩ
Normal Mode Noise Rejection:	Filtered 40 dB (minimum) @ 50, 60, 120, 240, 300, 400, & 420 Hz Unfiltered (3-pole active) 20 dB (minimum) above 50 Hz
Common Mode Noise Rejection: (to 1000V DC)	@ 80% R.H. 120 dB (minimum) from DC to 60 Hz with 100Ω in either lead 90 dB (minimum) from 60 Hz to 420 Hz @ 80 to 100% R.H. 90 dB (minimum) from DC to 60 Hz with 100Ω in either lead 60 dB (minimum) from 60 Hz to 420 Hz

Table 1.2 - Specifications continued

DC VOLTS (5 Ranges) (continued)	
Settling Time (unfiltered) to rated accuracy with step input involving: a. No range or polarity change b. Polarity and no range change c. Single up/ down range change	.1 and 1 range <4 seconds 10, 100, & 1000 range <500 msec
Settling Time (filtered) to rated accuracy:	.1 and 1 range <5.5 seconds 10, 100, & 1000 range 2 seconds

DC (3-WIRE) RATIO (5 Ranges)	
Full Range Display:	±.100000:1, ±1.00000:1, ±10.0000:1, ±100.000:1, ±1000:1 Readout is Ratio X10
Overrange:	100% on all ranges except ±1000 volts DC maximum input (signal)
Accuracy: (20°C to 30°C) to 70% R.H.	±0.01% of reading +0.005% of range x (Ref Rng + 10V/ Ref Input Voltage)
(0°C to 40°C) to 100% R.H.	±0.04% of reading +0.015% of range x (Ref Rng + 10V/ Ref Input Voltage)
(40°C to 55°C) Relative Humidity to decrease linearily from 100% @ 40°C to 20% @ 55°C	±0.04% of reading +0.015% of range x (Ref Rng + 10V/ Ref Input Voltage)
Voltage Range:	Signal Input – Numerator 0 to ±1000V DC Reference Input – Denominator +2V to +10.5V DC
Input Resistance: $\frac{\text{Signal Input}}{\text{Reference Input}}$	.01:1, .1:1, 1:1, 10:1 $\frac{100\ M\Omega}{1\ M\Omega}$ 100:1 $\frac{10\ M\Omega}{1\ M\Omega}$
Normal Mode Noise Rejection, Common Mode Noise Rejection, & Settling Time:	Same as DC Volts specifications

AC VOLTS (AVERAGING) (4 Ranges)	
Full Range Display:	1.00000, 10.0000, 100.000, and 1000.00V RMS
Overrange:	100% on all ranges except 1000 range, 1000 AC RMS volts to 20 kHz. Maximum input voltage x frequency not to exceed 2 x 10^7 volt-hertz
Resolution:	10 μV on the 1 volt range
Accuracy: (20°C to 30°C) to 70% R.H. for Short-Term Stability, 30 day	50 Hz to 20 kHz (100 μV to 500V AC) ±0.1% of reading + (±0.02% of range) 50 Hz to 20 kHz (500V to 1000V AC) ±0.15% of reading
(0°C to 40°C) to 100% R.H. for Long-Term Stability, 6 mo.	50 Hz to 20 kHz (100 μV to 500V AC) ±0.2% of reading +(±0.06% of range) 50 Hz to 20 kHz (500V to 1000V AC) ±0.25% of reading +(±0.06% of range)
(40°C to 55°C) Relative Humidity to decrease linearily from 100% @ 40°C to 20% @ 55°C for Long-Term Stability, 6 mo.	50 Hz to 20 kHz (100 μV to 500V AC) ±0.2% of reading +(±0.06% of range) 50 Hz to 20 kHz (500V to 1000V AC) ±0.25% of reading +(±0.06% of range)
Input Resistance:	2 MΩ in parallel with 100 pF
Common Mode Noise Rejection:	@ 80% R.H. 120 dB (minimum) from DC to 60 Hz with 100Ω in either lead 90 dB (minimum) from 60 Hz to 420 Hz @ 80 to 100% R.H. 90 dB (minimum) from DC to 60 Hz with 100Ω in either lead 60 dB (minimum) from 60 Hz to 420 Hz
Settling Time (Filtered) to rated accuracy with step input involving: a. No range change b. Single up or down range change	All ranges from 50 Hz to 20 kHz 3 sec + 1.5 sec filter settling time

Table 1.2 - Specifications continued

RESISTANCE (4-WIRE) (6 Ranges)	
Full Range Display:	.100000, 1.00000, 10.0000, 100.000, 1000.00, and 10000.0 KΩ
Overrange:	100% on all ranges Fault voltage, without damage: 30 volts DC or AC (RMS) all ranges KΩ source equipped with 20 mA fuse accessible from front panel
Resolution:	1 milliohms on the .1 KΩ range
Accuracy: **(20°C to 30°C)** **to 70% R.H.**	All ranges ±0.06% of reading +(±0.005% of range)
(0°C to 40°C) **to 100% R.H. for** **Stability, 6 mo.**	All ranges ±0.2% of reading +(±0.02% of range)
(40°C to 55°C) **Relative Humidity** **to decrease linearily** **from 100% @ 40°C** **to 20% @ 55°C-for** **Stability, 6 mo.**	All ranges ±0.2% of reading +(±0.02% of range)
Current Through Unknown:	.1 and 1 KΩ range 1 mA 10 KΩ range 100 μA 100 KΩ range 10 μA 1000 KΩ range (1 MΩ) 1 μA 10,000 KΩ range (10 MΩ) 100 nA
Open Terminal Voltage:	≤5 volts

RESISTANCE (4-WIRE) (6 Ranges) (continued)	
Settling Time (unfiltered) to rated accuracy with step input involving: **a. No range change** **b. Single up or down range change**	.1, 1, 10, 100, & 1000 ranges 1 second 10,000 range 5 seconds

SECTION 2 INSTALLATION & OPERATION

2.1 GENERAL.

2.1.1 This section covers the visual inspection, installation and storage of the Model 5100AF.

2.2 UNPACKING AND INSPECTION.

2.2.1 The instrument is enclosed between two molded, plastic-foam forms and packaged in a double-walled cardboard carton for shipment. The plastic forms hold the instrument securely in the carton and absorb any reasonable external shock normally encountered in transit.

2.2.2 Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the instrument from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3 POWER CONNECTIONS.

2.3.1 Power is supplied to the instrument through a standard 6-foot long detachable power cord. The ground pin (round) on the power plug is electrically connected to the power transformer primary winding shield and to the metal portion of the front panel. It is important that this pin be connected to a good quality earth ground.

2.3.2 The cord connects to the instrument at power input jack J201 on the rear panel.

2.3.3 The power fuse holder is located next to the power input jack and requires a .25 ampere fuse.

2.3.4 The instrument is designed to operate at one of two selectable line voltages; 115 or 230V AC.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

2.4 STORAGE REQUIREMENTS.

2.4.1 The instrument can be stored at temperatures ranging from $-40^{o}C$ to $+75^{o}C$ at 80% relative humidity without damaging the PCB's or components. The instrument must be brought up to operating range ($0^{o}C$ to $50^{o}C$) before power is applied.

2.5 RESHIPMENT PACKAGING REQUIREMENTS.

2.5.1 The shipping carton with its molded plastic foam forms and plastic dust cover is specifically designed to provide the required support necessary for safe shipment. Whenever possible, these should be used for reshipment.

2.5.2 If the original packing materials are not available, proceed as follows:

a. Wrap instrument in plastic or heavy paper.

b. Place packing material around all sides of instrument and pack in cardboard box.

c. Place instrument and inner container in a sturdy cardboard or wooden box. Mark box with appropriate precautionary labels.

SECTION 3 OPERATION

3.1 GENERAL.

3.1.1 This section presents instructions for operating the Model 5100AF Digital Multimeter. These instructions consist of preliminary checks and power up procedures followed by a description of the instruments controls and indicators. This is followed by a description of the operation for each function and instructions for connection of the instrument to the device under test.

3.2 OPERATION.

3.2.1 Before operating the instrument, it is strongly recommended that the operator read this entire section in order to avoid damage to the unit. After reading the operating instructions refer to the Installation Section, paragraph 2.3.4 and check the position of the line voltage selector.

> **CAUTION**
>
> This instrument may be damaged if operated on a line voltage other than that called for by the line voltage selection jumper.

3.2.2 After ensuring that the line voltage selector is in the proper position, connect the power cord to the power outlet and turn it on by depressing the POWER switch so that it is in the ON position as shown on the front panel. Allow the instrument to warm up for approximately one minute. When the instrument is turned on the display should light. The instrument is now ready for operation. Refer to the following paragraphs for details of control operation and measurement connections.

3.3 CONTROLS AND INDICATORS.

3.3.1 Function Select.

3.3.1.1 Four buttons select the functions: ACV, DCV, KΩ and RATIO. The AC, DC, and KΩ buttons are interlocked allowing only one button to be pressed at a time. Ratio is used in addition to DC for DC Ratio function.

3.3.2 Filter.

3.3.2.1 The filter button is a push on, push off switch that selects an active filter. The filter provides normal mode noise attenuation of > 30 dB at 50 Hz.

3.3.3 Range Select.

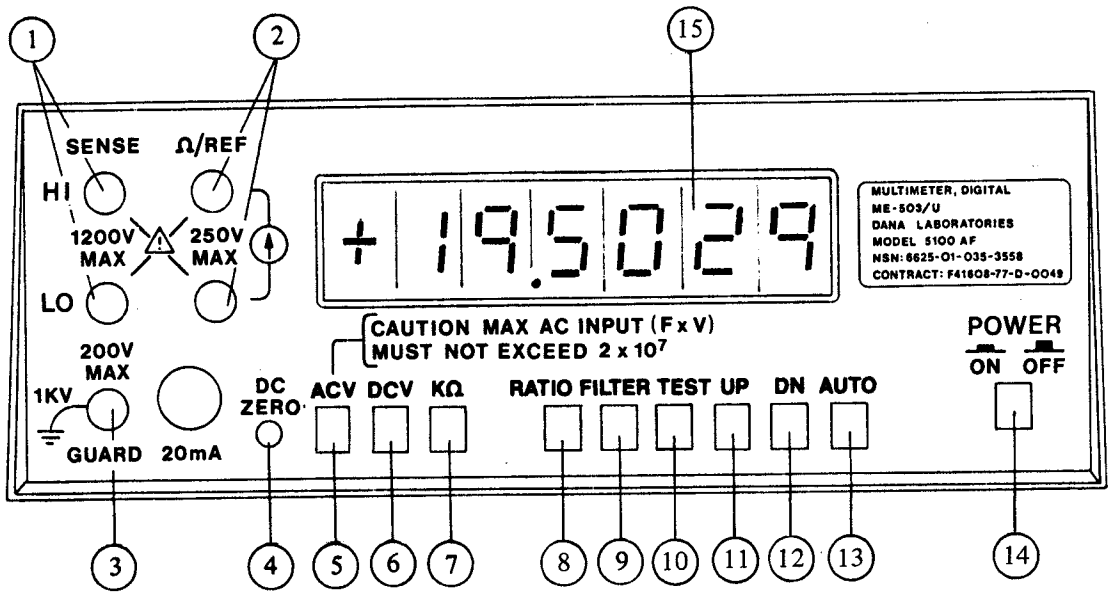
3.3.3.1 Three buttons are used to control ranging: AUTO, UP, and DN.

a. AUTO is a push on, push off switch. When pushed in, the instrument automatically selects the range most compatible with the input signal, the instrument up ranges at 100% of range and down ranges at 10% of range.

b. UP button is a momentary switch. UP range occurs one range at a time with each depression of the button when DMM is in non-auto range position.

c. DN button is a momentary switch. DN range occurs one range at a time with each depression. Will also operate in auto range mode if one needs to go down range between 60% and 20%.

Table 3.1 - Front Panel Identification



(1) Voltage Input, Ohms Sense Terminals

(2) Ohms Current, Ext Ref Input Terminals

(3) Guard Terminal

(4) DC offset. Allows user to zero front panel display

(5) AC Volts Function Select Switch, push on

(6) DC Volts Function Select Switch, push on
Used with (8) for DC Ratio X10

(7) KOHMS Function Select Switch, push on

(8) RATIO Function Select Switch, push on
Used with (6) for DC Ratio X10

(9) FILTER Select Switch, push on, push off

(10) TEST switch, push on.

(11) UP. Causes instrument to up range. Momentary on

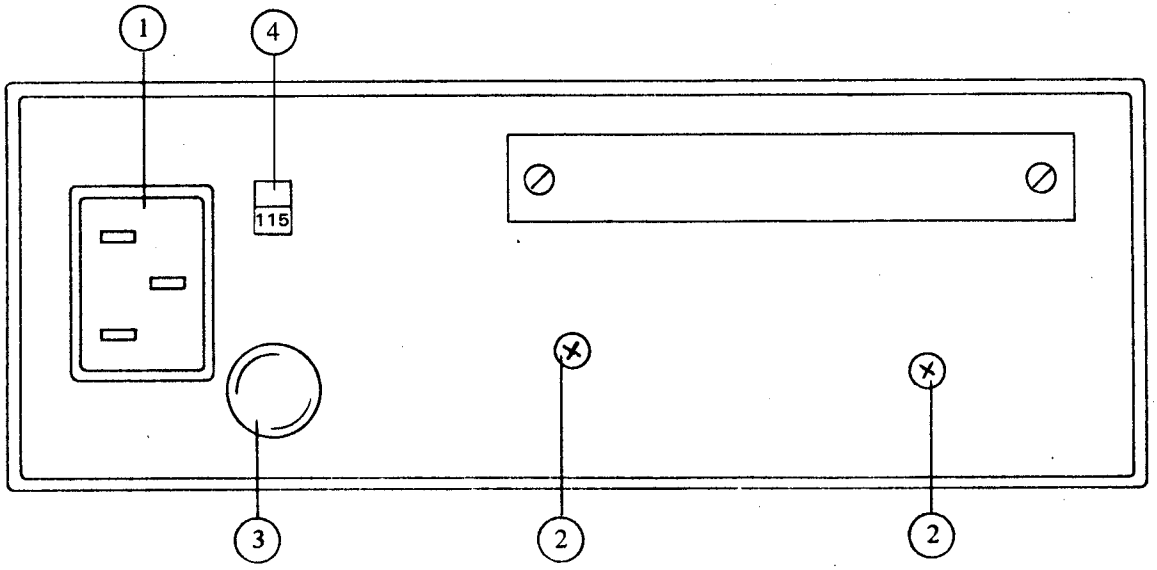
(12) DOWN. Causes instrument to down range. Momentary on

(13) AUTO. Selects range most compatible with input signal. Push on, push off

(14) POWER Switch. Push on, push off

(15) DISPLAY. Consists of 6 decade readouts "0 – 9" and a ± readout

Table 3.2 - Rear Panel Identification



(1) Power Receptacle J201 receives power cable.

(2) Disassembly Screws (2). Removal of these screws allows removal of case.

(3) Power Fuse Holder F201.

(4) Line Selector Switch S201.

3.3.4 Power.

3.3.4.1 The power switch is a push on, push off switch. When on, power is applied to all circuits.

3.4 DISPLAY.

3.4.1 The Display consists of six numeric LEDs, .43 inches high, and a polarity LED.

3.5 MEASUREMENT CONNECTIONS.

CAUTION

The maximum AC input voltage is 1000V @ 20 kHz.

3.5.1 For basic voltage measurements, an ac or dc voltage measurement connection recommended to minimize the effects of noise requires a two-conductor shielded cable connected as shown in figure 3.1.

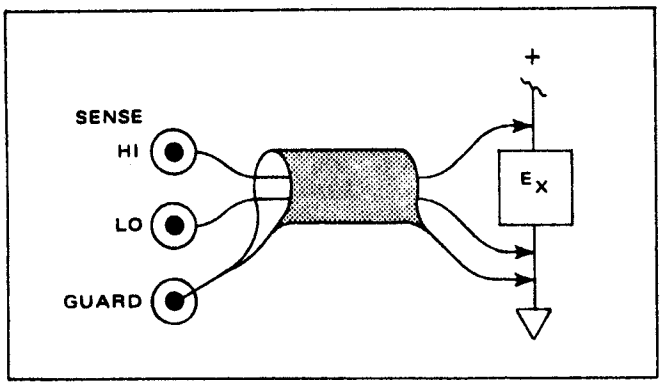


Figure 3.1 - Basic Voltage Measurement Connections

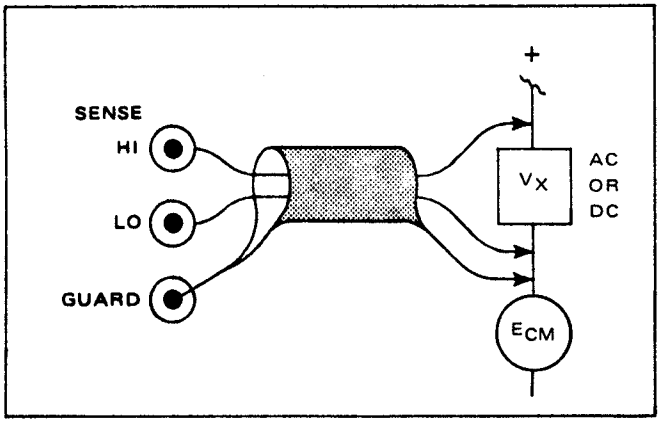


Figure 3.2 - Connections where CM Present

3.5.2 For all voltage measurements, the GUARD lead and LO lead are connected to the measurement point nearest ground potential. Somewhat less shielding is achieved by placing a jumper between LO and GUARD. This arrangement is adequate for measuring all but low voltage (mV) levels and/or in high-noise environments. When making measurements of low voltage levels in noisy environments or where common mode signals are present it is recommended that the two-wire-shielded type of input cable be used. This input configuration is shown in figure 3.2.

The option 80 input cable is especially useful in low signal high noise applications.

3.5.3 When making "floating" voltage measurements (both measurement points above ground potential), do not connect GUARD to measurement ground without making sure that the voltage between GUARD and LO does not exceed 200 volts.

3.5.4 Ohms Measurement.

3.5.4.1 Ohms measurement consists of the application of a fixed value of current through the unknown resistor, supplied through the HI and LO Ω current terminals. The resulting voltage drop is measured by the DMM through the HI and LO SENSE terminals. The current is set for each range at a level that produces a full scale reading when the unknown resistor is the same as the range selected (i.e., a 1 Kohm resistor measured on the 1 Kohm range produces a full scale reading of 1.00000).

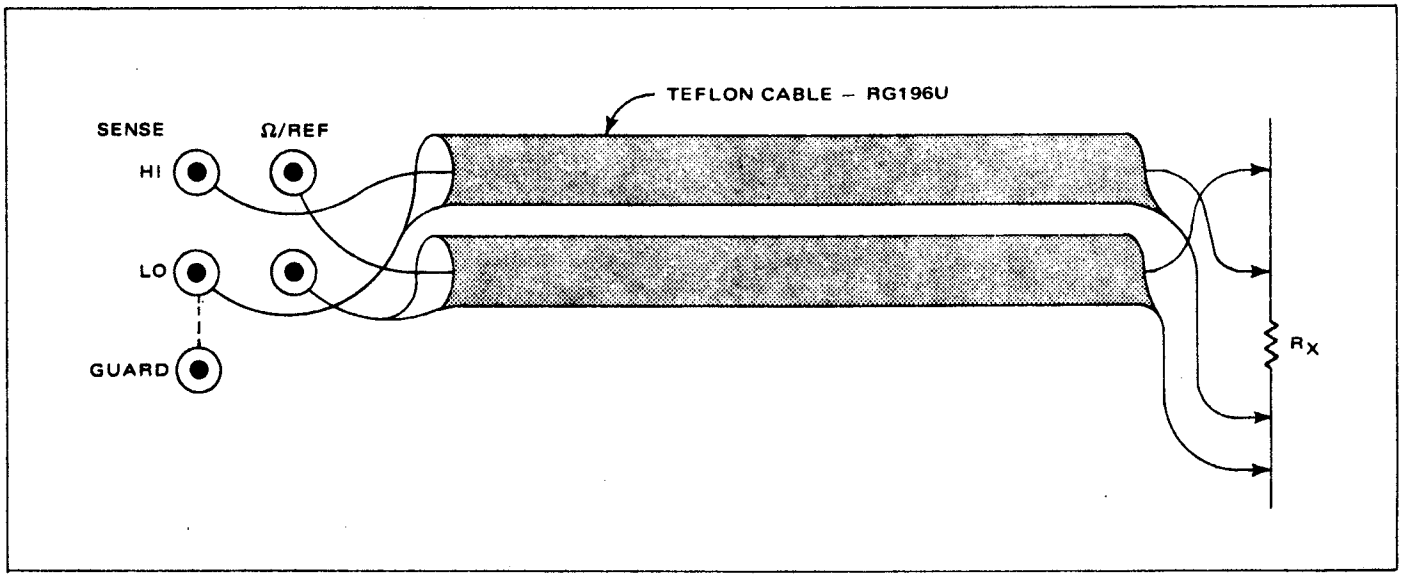


Figure 3.3 - Ohms Measurement Connection

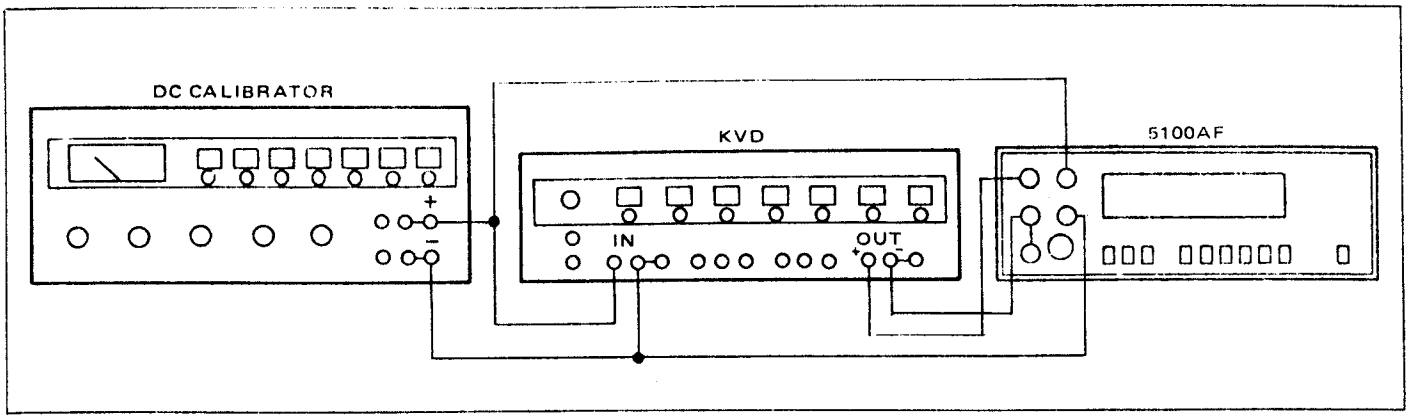


Figure 3.4 - 3-Wire Ratio X10 Measurement Connections

3.5.4.2 Connecting the instrument to a resistor for ohms measurement consists of connecting both the HI Ω current and HI SENSE terminals to one side of the resistor and both the LO Ω current and LO SENSE terminals to the other side of the resistor. An example is shown in figure 3.3.

3.5.5 DC Ratio Measurements.

3.5.5.1 A 3-wire DC Ratio X10 capability is configured when the DCV (S2) and Ratio (S5) switches are enabled. The shorting links between J101 and J103 or J102 and J104 must be removed before signal and external reference voltages can be connected to the DMM. Ratio ranges of .01:1 (.1 signal range) to 100:1 (1000 signal range) can be obtained with signal (numerator) inputs of either polarity. External reference (denominator) inputs of +2 to +10 volts are used to replace the internal +1V reference in the 3-wire ratio technique. An external reference voltage of +2 volts will produce a ratio readout percent of range accuracy five times less than that of a +10 volt external reference. This can cause a greater amount of run-around which may require the use of the measurement filter (S6) to produce qualitative ratio data.

A full scale signal input, for example, of +1V and an external reference input of +5 volts may exceed 200000 counts which will require a manual uprange change to the 10 range or switching to the autorange.

A sound practice is to use the DCV function to measure the signal and reference voltages to see that they conform to the limitations of a 3-wire ratio technique before the actual measurement hookup is made. When the input signal to be measured is negative, avoid ground loops and unreferenced power levels to prevent potential shock hazards and possible damage to associated test equipment. Floating 3-Wire Ratio X10 measurements should not be attempted.

An example of a 3-Wire Ratio X10 signal and reference connections are shown in figure 3.4.

3.5.6 Current Measurement.

3.5.6.1 The Model 5100AF may be used to measure AC or DC current if used with option 85 current shunts. In operation the shunt for the desired current range is plugged into the HI and LO input terminals. The test lead set or input cable is then plugged into the shunt and connected to the measurement circuit.

SECTION 4 THEORY OF OPERATION

4.1 INTRODUCTION.

4.1.1 This section describes the operation of the Model 5100AF DMM and includes the basic technique used as well as a more detailed explanation of the major functional portions.

4.2 CIRCUIT DESCRIPTION.

4.2.1 A functional block diagram of the instrument is presented in figure 4.1. The diagram is divided into four major areas for purposes of discussion; (1) Signal Conditioning, (2) Digitizing, (3) Ranging, and (4) Display. Measurement signals applied to the input terminals are routed to the appropriate signal conditioning device by the function controls. Because the isolator amplifier operates with low voltages, dc measurement signals higher than 2 volts must be scaled down. This is accomplished by the attenuator. The attenuator also changes the source current flow on the ohms ranges. The ac converter contains its own voltage attenuator for the ac voltage ranges above 2 volts.

4.2.2 The ac converter produces a dc output level proportional to the ac measurement applied to its input. On the ac ranges this dc signal is applied to the isolator.

4.2.3 The ohms amplifier provides a constant current source to the front panel source terminals. The current flows through the resistance being measured on the Kohms function and the resultant voltage developed across the resistance is directly proportional to the resistance value. The voltage across the resistance is measured and displayed by the instrument as the value of the resistance in ohms.

4.2.4 The isolator functions as a buffer to prevent application of "normal-mode" noise or "common-mode" voltages to the integrator circuit. It also serves to provide a high input impedance on the low voltage dc ranges of the instrument. The output of the isolator is applied to the integrator for conversion to a digital count.

4.2.5 The integrator is a dual-slope conversion device which charges a capacitor for a fixed time period to a level which is dependent upon the level of the measurement signal (see figure 4.3). The capacitor is then discharged at a fixed rate by switching a reference signal of opposite polarity onto the input of the integrator. As the capacitor discharges it crosses the zero volt level and begins to charge in the opposite direction. A null detector in the integrator circuit senses this zero-crossing and produces a "null-detect" signal. The null detect signal is used by the Timing and Control circuits to stop the measurement counter. Thus, the count value in the measurement counter is a direct digital representation of the measurement signal voltage applied to the instrument.

4.2.6 The Timing and Control circuits provide the integrator and counter with the synchronization required to perform the analog to digital conversion of the measurement signal. The instrument performs continuous measurement cycles. The measurement cycle is illustrated in figure 4.2.

4.2.7 Note that the digitize cycle is divided into four major periods. The first, which is 50 milliseconds long, is the signal integrate period. During this time the Timing and Control circuits apply the measurement signal to the input of the integrator. The integrator, during this period, charges a capacitor to a level determined by the value of the measurement signal. During the next period the Timing and Control circuits apply a reference voltage opposite in polarity to the measurement signal to this capacitor in order to discharge it. The capacitor is discharged at a fixed rate and as the charge on the capacitor reaches zero the integrator produces a null detect signal which is used by the Timing and Control circuits to stop the count in the measurement counter. Thus, the value of the count in the measurement counter is directly proportional to the value of the measurement signal. During the signal integrate period the Timing and Control circuits detect the polarity of the measurement signal and store this information in a flip-flop.

4.2.8 The measurement counter is a special integrated circuit chip which includes the measurement counter, a latch to store the count, a decoder, and multiplexer. The measurement count stored in the latch is in BCD code and must be converted to a 7-line code for application to the LED display. This is accomplished by the 4-to-7 line decoder. The multiplexer, in the measurement counter, transfers one digit of information at a time from the latch to the 4-to-7 line decoder. The 7-line code from the decoder is applied to all of the LED display digits in parallel. The MUX switching line turns on each LED digit as its code appears on the output of the 7-line decoder. Thus, the LED display devices are actually flashing in sequence but the display rate is of a frequency that makes the LEDs appear to be continuously illuminated.

4.2.9 Range control is accomplished either manually from the front panel or automatically by the internal range control logic. There are three switches on the front panel of the instrument labeled UP, DOWN, and AUTO. If the operator desires to use the auto ranging feature he simply pushes in the Auto pushbutton (a latching type switch). If it is desired to use manual range control the Auto range switch is unlatched and the operator then has control through use of the UP and DOWN pushbuttons. The range control logic configures the voltage attenuator to scale

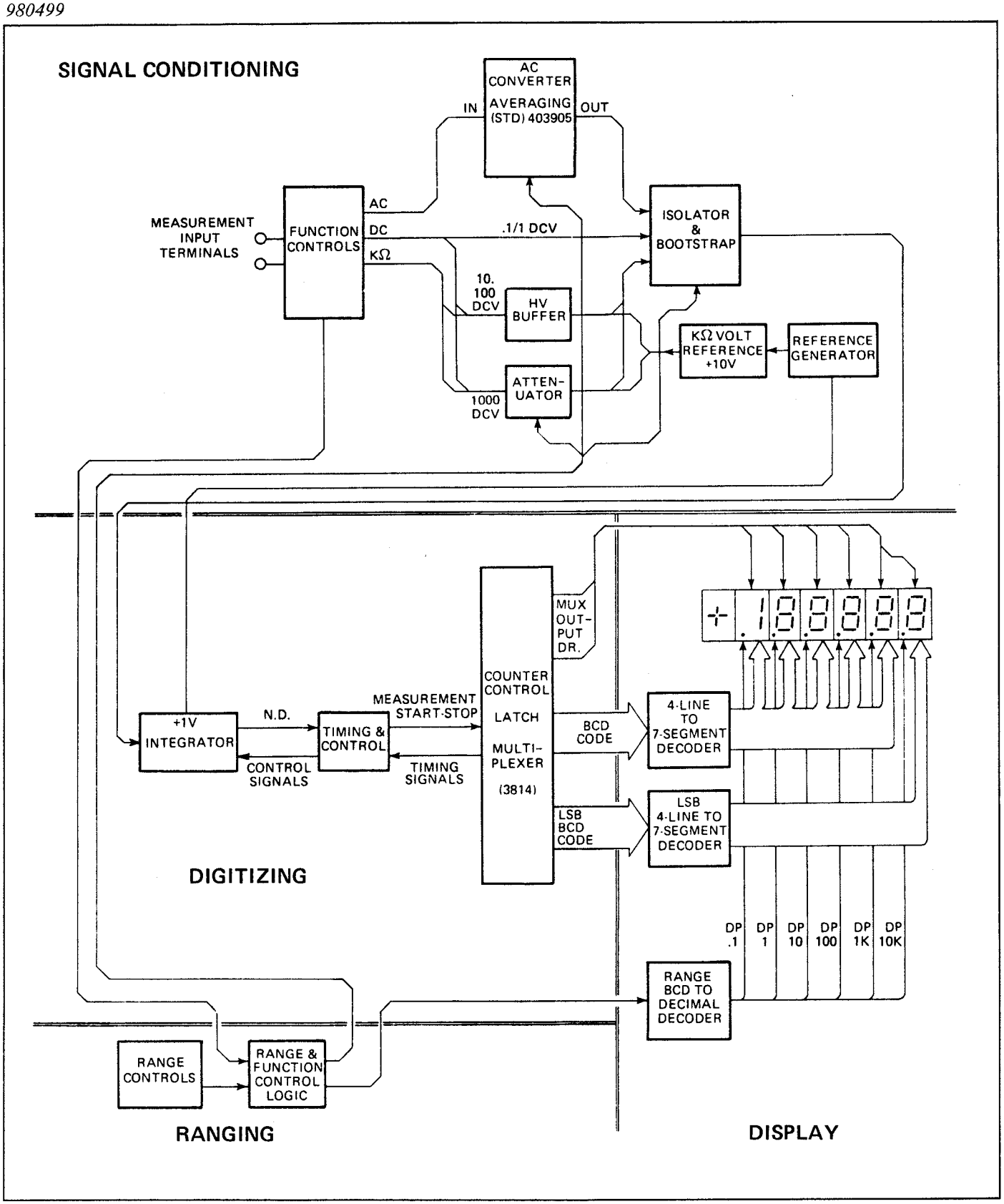


Figure 4.1 - Functional Block Diagram

down measurement input signals. In addition, it controls the attenuator in the AC Converter circuit. The isolator gain is also controlled by the range control logic and is switched from X1 to X10 gain, depending on the selected operating range of the instrument. The range code from the range control logic is applied to the decimal decoder which provides the signals to the LED displays to properly locate the decimal point.

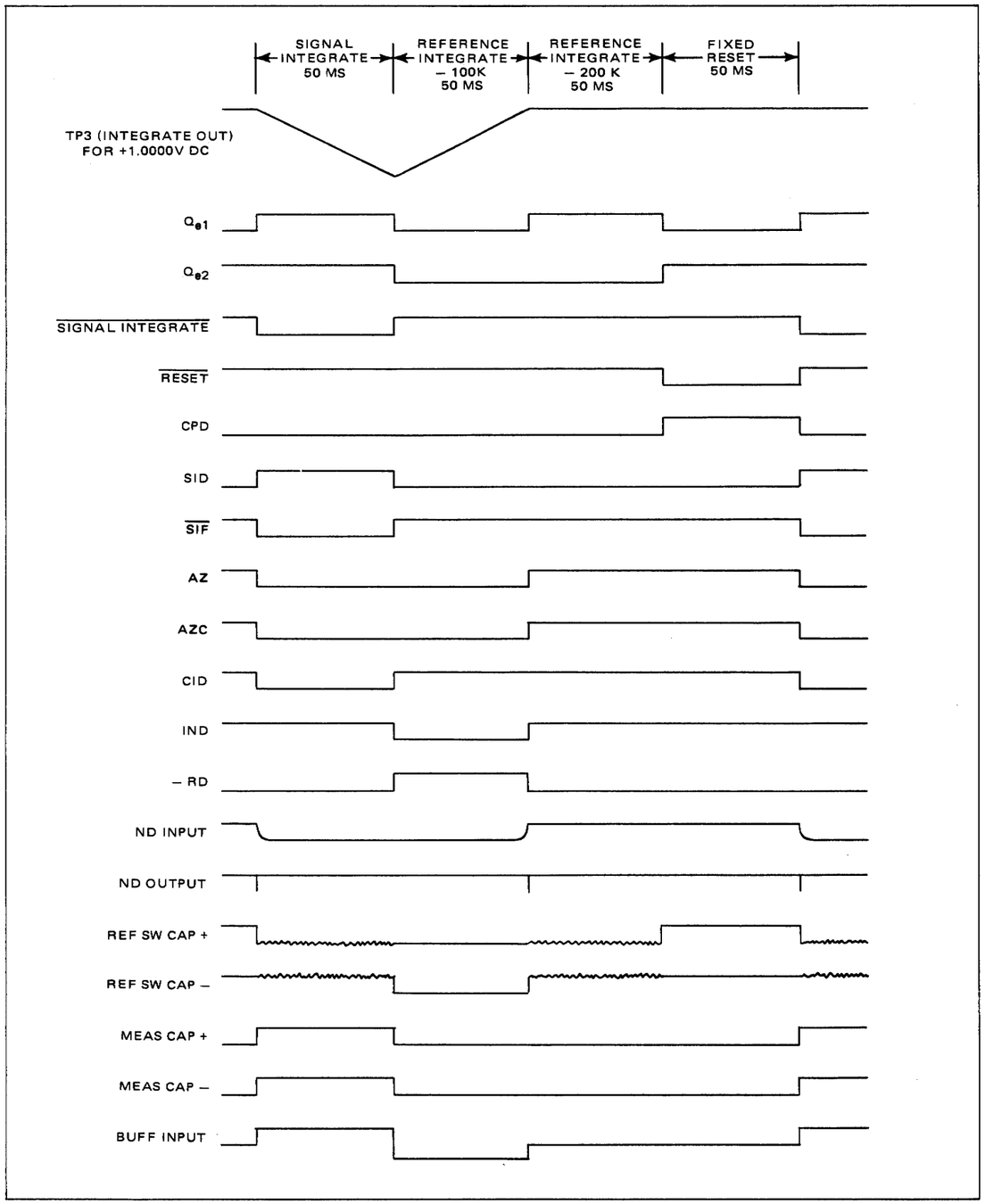


Figure 4.2 - Measurement Cycle

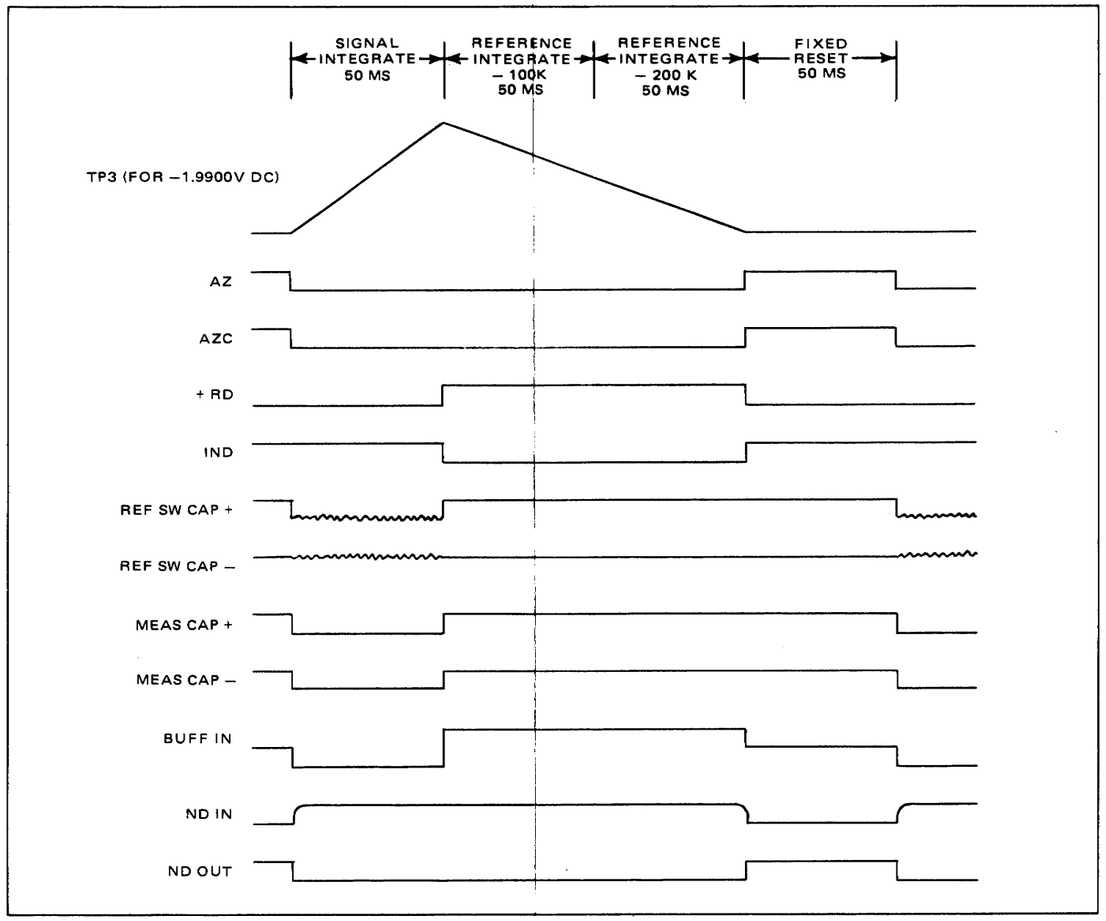


Figure 4.2 - Measurement Cycle continued

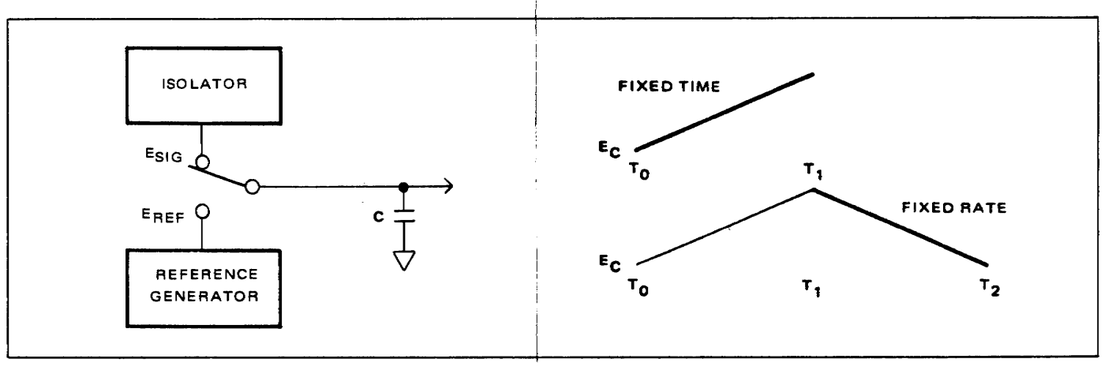


Figure 4.3 - Dual Slope Integration

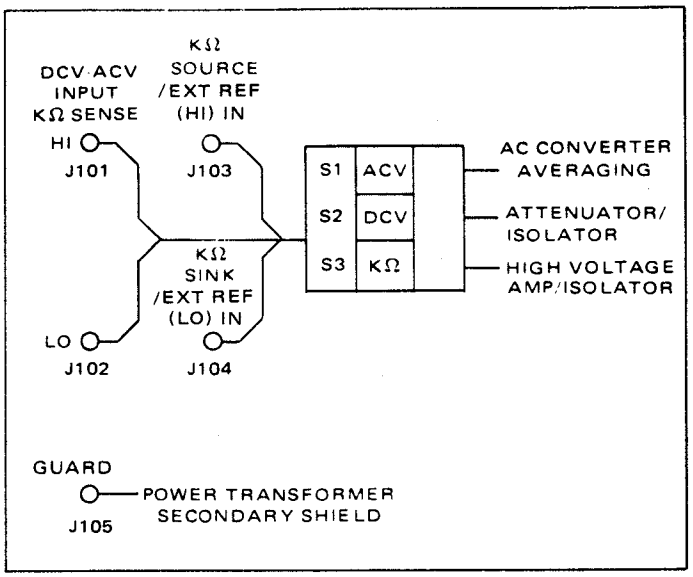


Figure 4.4 - Function Controls

4.3 DETAILED CIRCUIT DESCRIPTION.

4.3.1 The following paragraphs present the detailed description of the individual functional circuits of the instrument. The circuit descriptions are arranged in the order that they appear on the overall block diagram, figure 4.1.

4.3.2 Note that the schematic diagrams in the Drawing Section (Section 6) of this manual contain outlines of the components included in a functional circuit group. These outlined areas contain the same title of the blocks shown in diagrams in the Theory Section.

4.3.3 Function Controls.

4.3.3.1 A simplified block diagram of the function controls is illustrated in figure 4.4. The function controls consist of

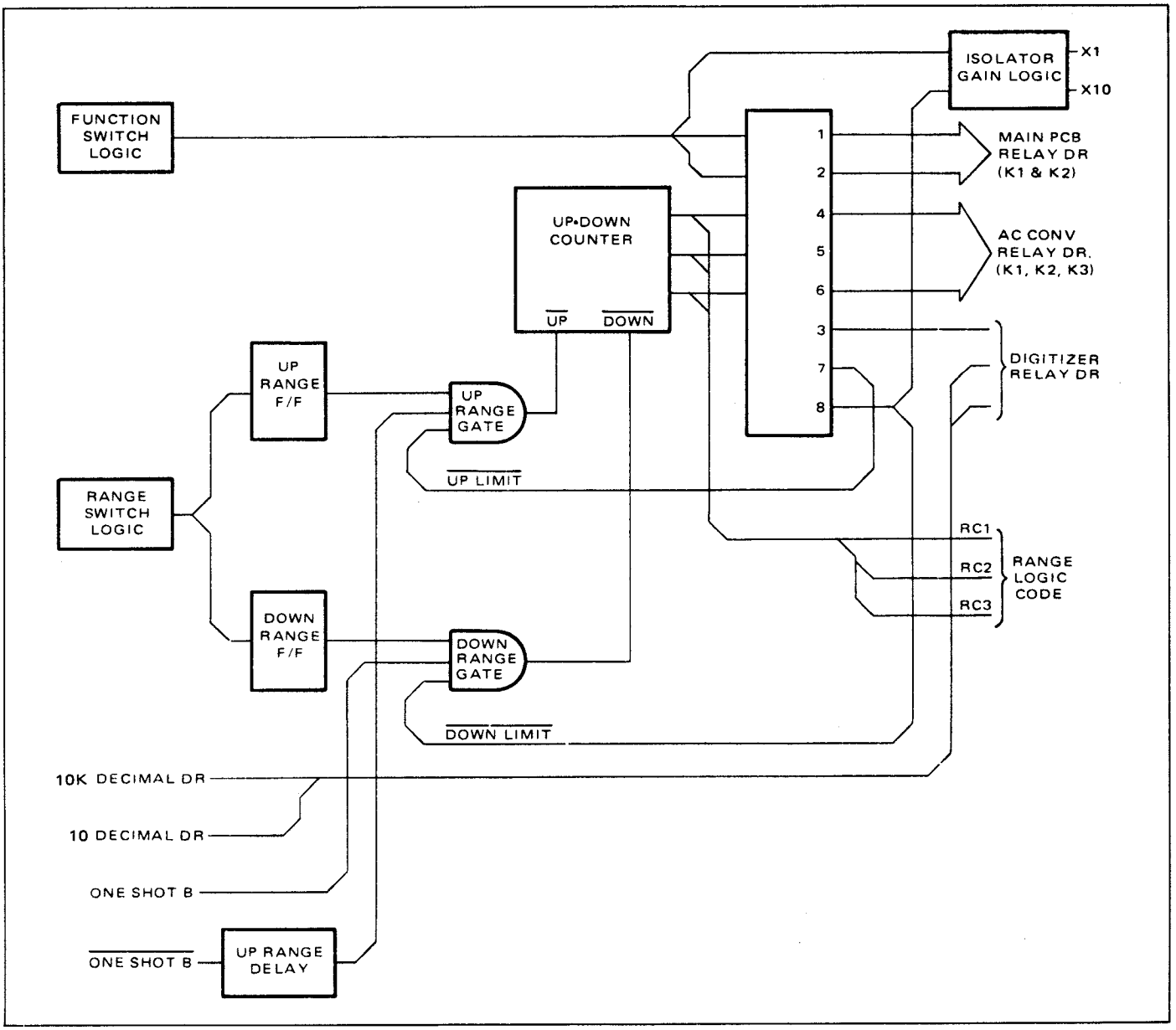


Figure 4.5 - Function and Range Logic

front panel pushbuttons labeled AC Volts, Kohms, DC Volts, and Ratio. Note that there are two sets of input terminals for applying measurement signals to the input of the instrument. One set is used to provide the full scale current for resistance measurements and, also, to provide the External Reference input voltages for Ratio. The other set of input terminals is used for measuring dc volts, ac volts and Kohms. The four function control switches route the input measurement signal through one of three paths when making a measurement of either voltage. The measurement signal is routed from the input terminals to the input of the AC Converter. When making dc voltage measurements the measurement signal is applied to the input of the isolator and, in like fashion, the ohms measurement signal is routed to the input of the ohms circuits. Although the block diagram shows that the measurement signal is applied to the input of one of these three circuits, measurement signals are actually routed through the voltage attenuator circuits for prescaling purposes. This is discussed in more detail in the following paragraph.

J101 – + IN ACV DCV (KΩ with addition of J103)
J102 – – IN ACV DCV (KΩ with addition of J104)
J103 – KΩ (with J101) & RATIO (Ext Ref Hi In)
J104 – KΩ (with J102) & RATIO (Ext Ref Lo In)
J105 – GUARD to be connected to J102 for all measurements except floating inputs

4.3.4 Range Control Logic.

4.3.4.1 The range control logic is illustrated in simplified form in figure 4.5. The range control circuits control the gain of the isolator, the attenuation in the AC Converter and in the voltage circuits. In addition, the range control circuits provide a range code to the decimal decoder for positioning of the decimal point on the front panel display. The heart of the range control circuits is the range counter, a three state UP/DOWN counter controlled by a pair of UP/DOWN flip-flops. When the range is to be stepped up manually the switch closure from S8-B in combination with the clock applies a pulse to the UP input of the range counter, thereby increasing the count. Manual down ranging is accomplished in exactly the same way by a switch closure from S9-A when the DOWN pushbutton is depressed. In auto range, the same UP or DOWN flip-flops are set by two signals which come from the counter. If the counter reaches a count which is greater than 100% of the measurement count prior to the null detect it produces an overload (O/L) signal. This signal is applied to the step-up flip-flop and causes the range counter to step up one count. If the null detect signal should occur before the counter reaches the 10% point in its count a signal termed divide by 2K (÷2K) is produced indicating that the measurement is less than 10% of full scale. This divide by 2K signal is applied to the step-down flip-flop, which causes the range counter to count down one step. Thus, the manual pushbuttons, or the internal logic, cause the range counter to step to the proper range and produce the range codes RC1, RC2, and RC3. The range code is applied to the decimal decoder to locate the decimal point on the front panel display. In addition the range codes are applied to the read-only memory, which is configured by internal firmware, to produce relay control signals which configure the attenuator relays. The isolator gain is controlled by the range counter, read-only memory, and by the switch positions of the function control switches on the front panel.

4.3.5 AC Converter (Averaging).

4.3.5.1 The AC Converter is shown in simplified form in figure 4.6. As shown on the diagram, it consists of an input attenuator network, a rectifier amplifier, and an output filter. The input attenuator network serves to scale down the input measurement voltage controlled by the range relays K1, K2, and K3. The 1V range attenuation is controlled by the fixed R/C values of the input circuit and the input voltage is applied directly to the rectifier amplifier. On the 10, 100, and 1000 ranges, relays K1, K2, and K3 are respectively energized to provide the proper signal input attenuation. The ACV Function configures the isolator for a fixed gain of 1 for all ranges. The rectifier amplifier consists of a dual FET input stage that feeds an operational amplifier that drives a G_m stage and two rectifier feedback diodes that convert the input measurement signal to a dc voltage, which is smoothed by an output filter network.

4.3.6 High Voltage Buffer.

4.3.6.1 The high voltage buffer is illustrated in simplified form in figure 4.7. This circuit protects the isolator from high measurement voltages, presents a high impedance to the measurement circuit to prevent circuit loading and isolates the KΩ source terminal from the attenuator reference bridge on all KΩ ranges.

In operation the two transistors (diode connected) Q1 and Q2 serve as an input clamp to prevent application of excessive voltage to the high impedance buffer Q4. The high impedance buffer is a dual FET device configured with the amplifier AR1 to form a unity gain amplifier of extremely high impedance.

The output of the AR1 is routed through the 1000 KΩ resistor to the attenuator and from the attenuator to the isolator.

In the Kohms function, the output of the AR1 is routed to the reference common line (refer to figure 5.16, KΩ Single Thread Diagram, upper right quadrant). The output of the high voltage buffer AR1 raises the reference common voltage as current is drawn from the ohms source terminal so that the current flow is constant through the resistance being measured Rx.

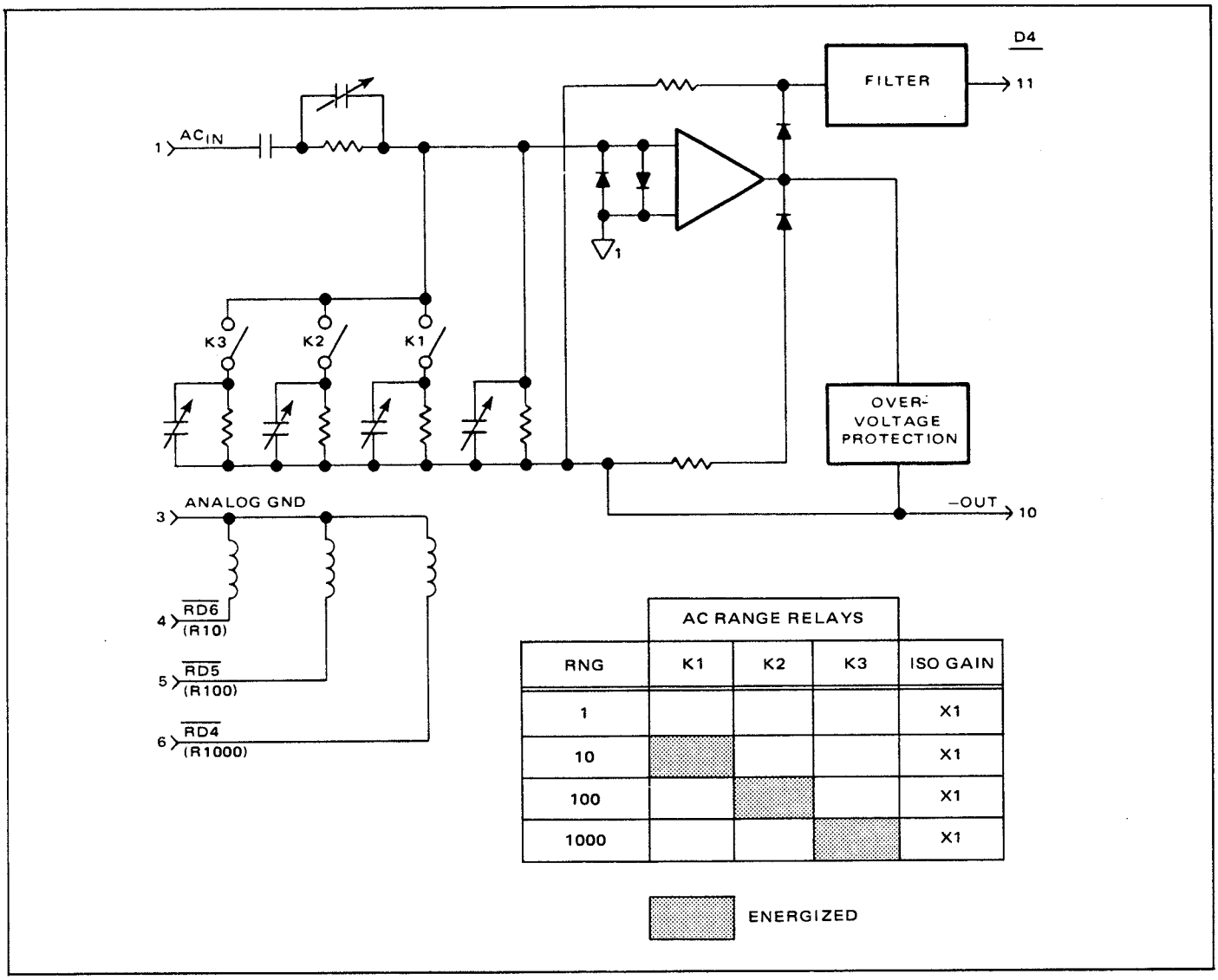


Figure 4.6 - Averaging AC Converter

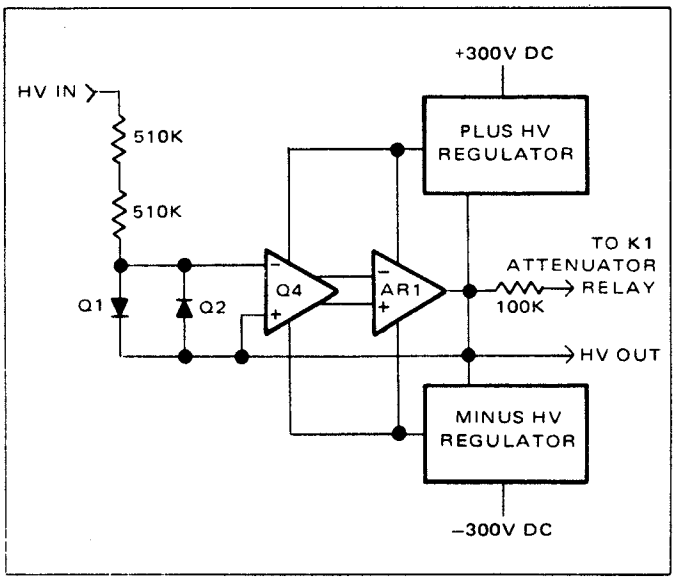


Figure 4.7 - High Voltage Buffer

4.3.7 Attenuator.

4.3.7.1 This circuit is shown in simplified form in figure 4.8. The attenuator performs the following functions; 1) attenuation of input measurement voltages on the 10, 100, and 1000 volt dc ranges, 2) scales down the ohms current source when the instrument is on the Kohms ranges, and 3) the attenuator contains a series resistance string with pick-off points selected by range relays. The attenuator, in the 10 and 100 DCV ranges, divide the HV Buffer output by 10:1 and 100:1, respectively, to provide full scale inputs to the isolator of ±1V DC. The attenuator, for the 1000 range, is preceded by a 9 MΩ resistor on the main PCB to provide a 1000:1 reduction in voltage from the measurement input to the isolator input.

When configured in the KΩ ranges, the attenuator uses the resistor elements in series with the KΩ reference generator

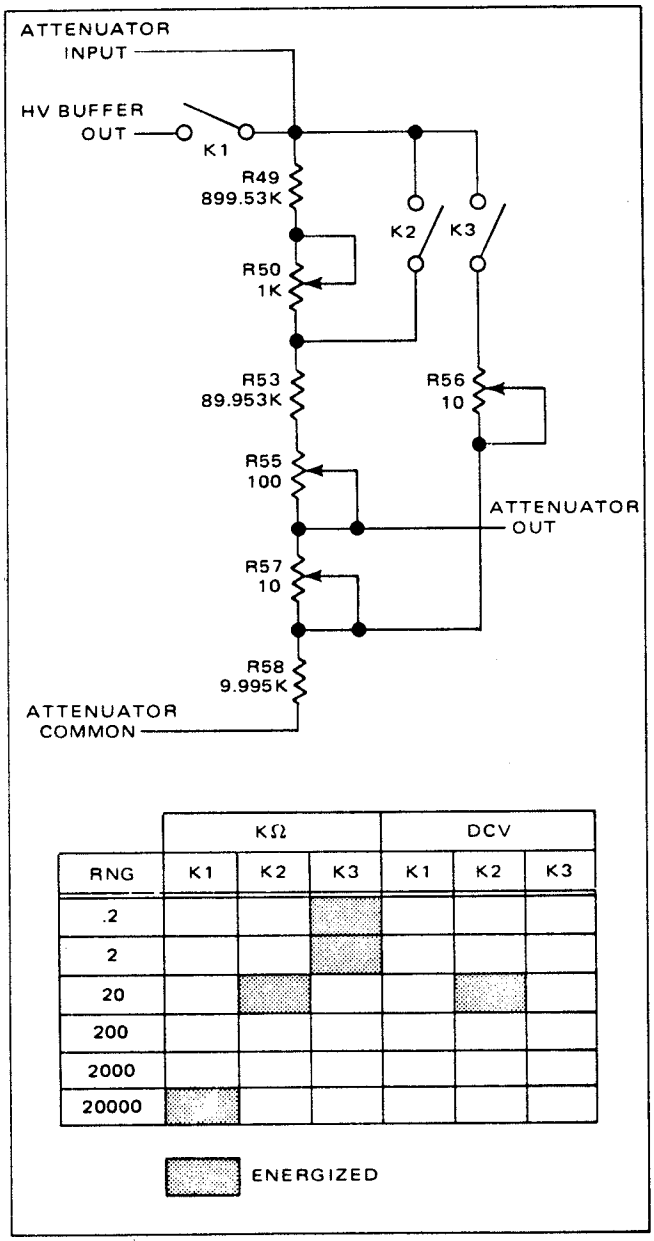


Figure 4.8 - Attenuator

voltage (+10V DC) to provide the required full scale currents at the KΩ source input terminal, J103. The 9 MΩ main PCB resistor is configured with the attenuator and HV Buffer in the 1000 KΩ and 10,000 KΩ ranges.

4.3.8 Isolator.

4.3.8.1 The isolator, shown in figure 4.9, consists of an input clamp, an isolator amplifier, a bootstrap amplifier, and a gain switching network. The various prescaled and processed input measurement voltages are applied to the input of the isolator which is clamped to prevent application of more than ±5V to the input of the isolator amplifier. The isolator amplifier is an operational amplifier with a gain of 1 or a gain of 10, depending upon the control signals applied to the gain switches by the range control logic of the instrument. The isolator accepts either positive or negative voltage levels at its input on one of two ranges; 1) zero to .1999 volts or 2) zero to 1.99 volts. Because of the gain switching, controlled by the range control logic, the output of the isolator is always zero to 1.999 volts dc. Note that the negative and positive supply voltage for the isolator amplifier is supplied by the bootstrap amplifier. These voltage sources are labeled + bootstrap voltage (+ BSV) and – bootstrap voltage (– BSV). The purpose of the bootstrap amplifier is to provide the isolator amplifier with a supply voltage which is always centered about the input measurement signal to the isolator amplifier. The +BSV voltage is always 5 volts higher than the input signal and the – BSV is always 5 volts lower than the input signal voltage. Thus, the isolator amplifier is always supplied with source voltages centered around the input signal. This combination provides high input impedance to avoid loading the circuit under test. The current sink AMP circuit, at the output of the isolator, provides a voltage, i.e., current, equal and opposite to the isolator output. This effectively raises the input impedance of the signal "low" input terminal by cancelling the effects of signal current errors from the measurement input to the integrator.

4.3.9 Reference Generator.

4.3.9.1 The reference generator produces the accurate one-volt to the digitizer circuits for measurement of AC and DC voltages. It also furnishes a 10 volt reference voltage to ohms reference circuit for use in the ohms measurement functions. The reference generator is shown in simplified schematic form in figure 4.10 and in complete schematic form on sheet 2 of drawing number 432104, page 6-15.

The circuit consists of a resistance bridge, an operational amplifier, transistor Q10, and reference zener CR10.

In operation the zener presents approximately 6.3 volts at the – input of AR4 maintaining a stable 10 volt DC output at Q10. The resistor network around CR10 consisting of resistors R39, R40, R41, R42, R45, R46, R50, and R51 is designed to operate the reference zener at a current which produces the highest voltage stability over a wide temperature range. These resistors are factory-selected-value (FSV) resistors and the schematic shows only nominal values. In addition some of the resistors may not be installed in some instruments.

The resistance bridge contains two potentiometers for adjusting the one volt and 10 volt output voltages.

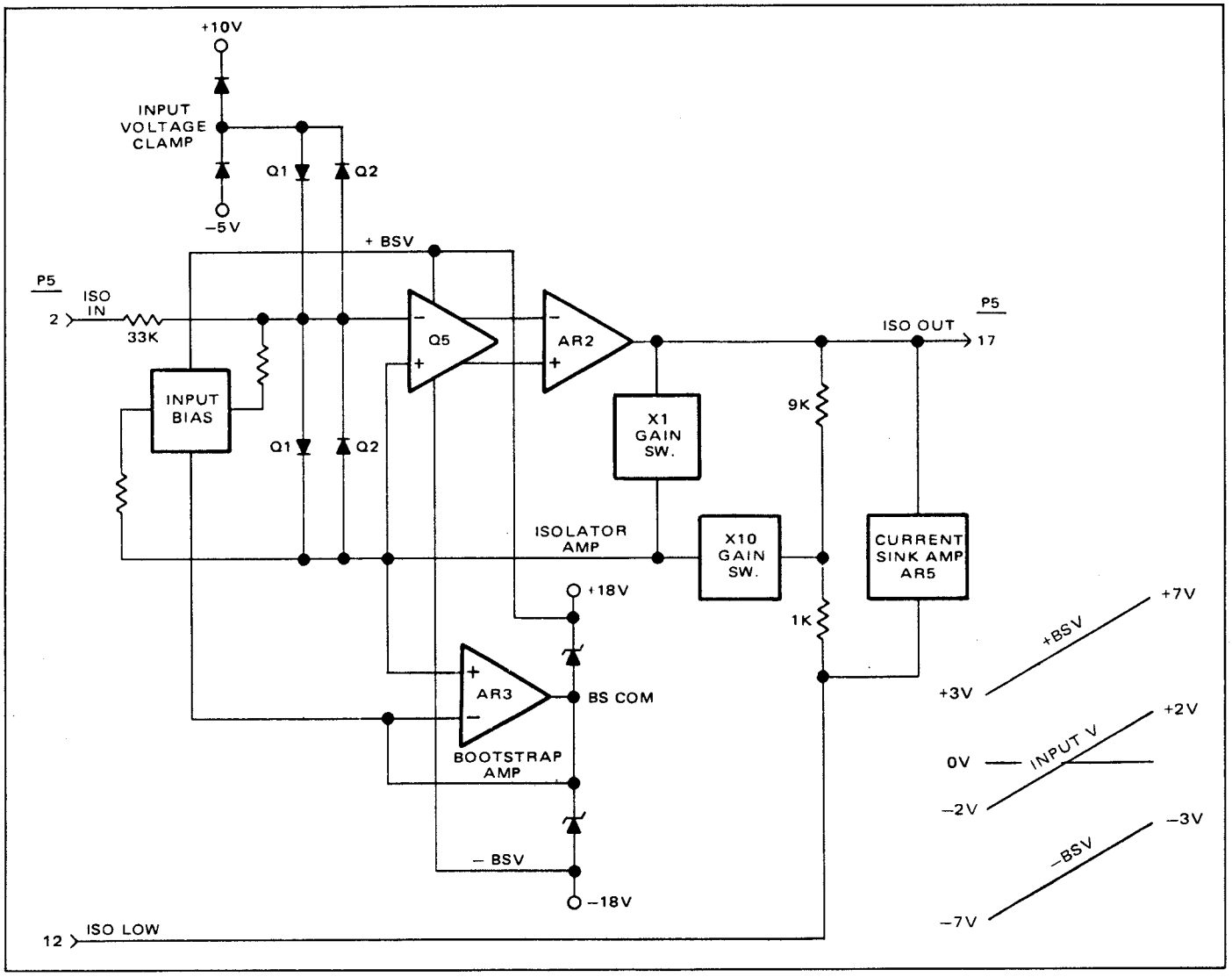


Figure 4.9 - Isolator & Bootstrap

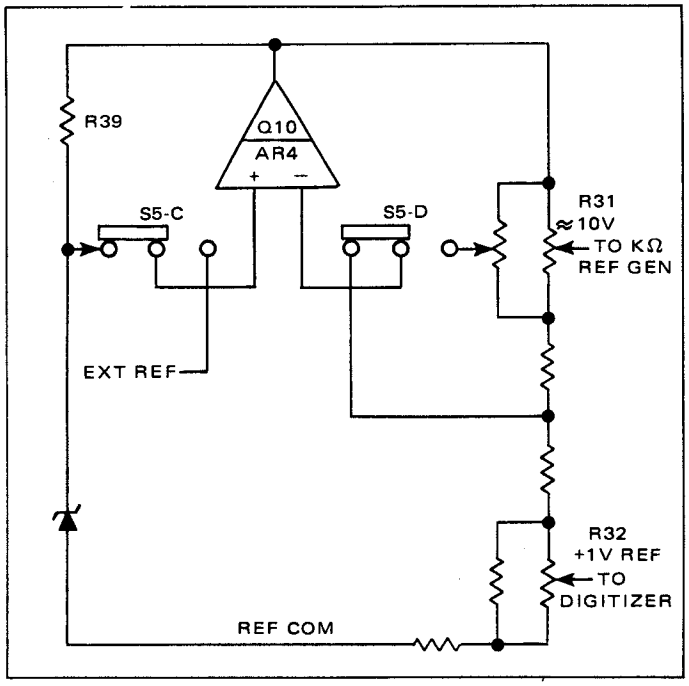


Figure 4.10 - Reference Generator

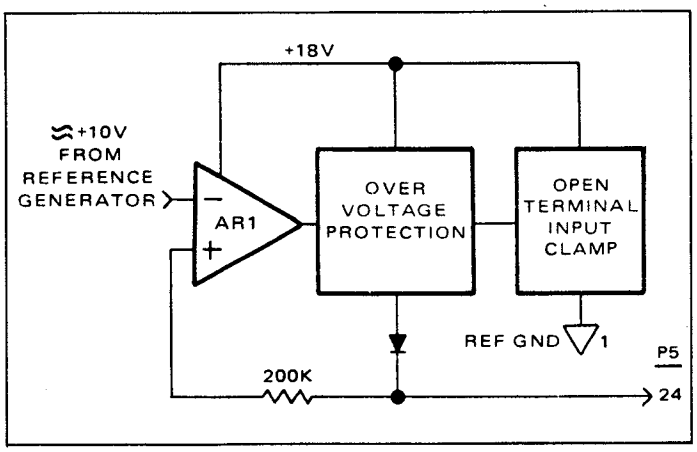


Figure 4.11 - KΩ Reference Generator

4.3.10 KΩ Reference Generator and Overvoltage Protection Circuit.

4.3.10.1 The KΩ reference generator provides a stable 10 volt reference voltage for application to the ohms source terminal via the attenuator circuit. The circuit is shown in simplified form in figure 4.11 and schematically on sheet 2

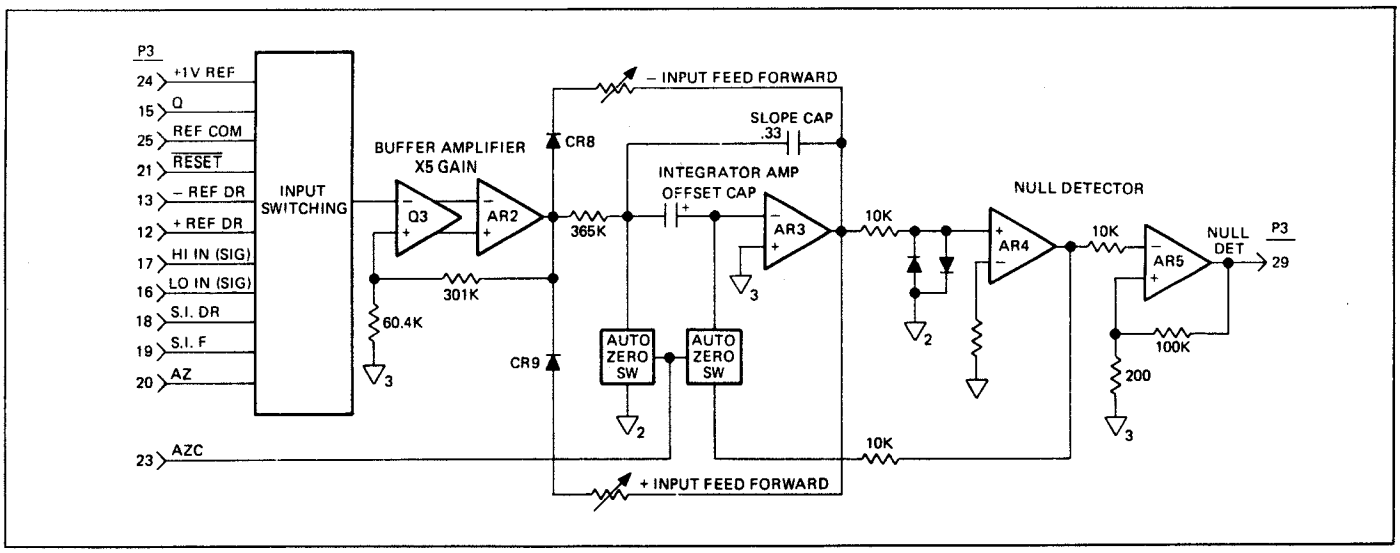


Figure 4.12 - Digitizer

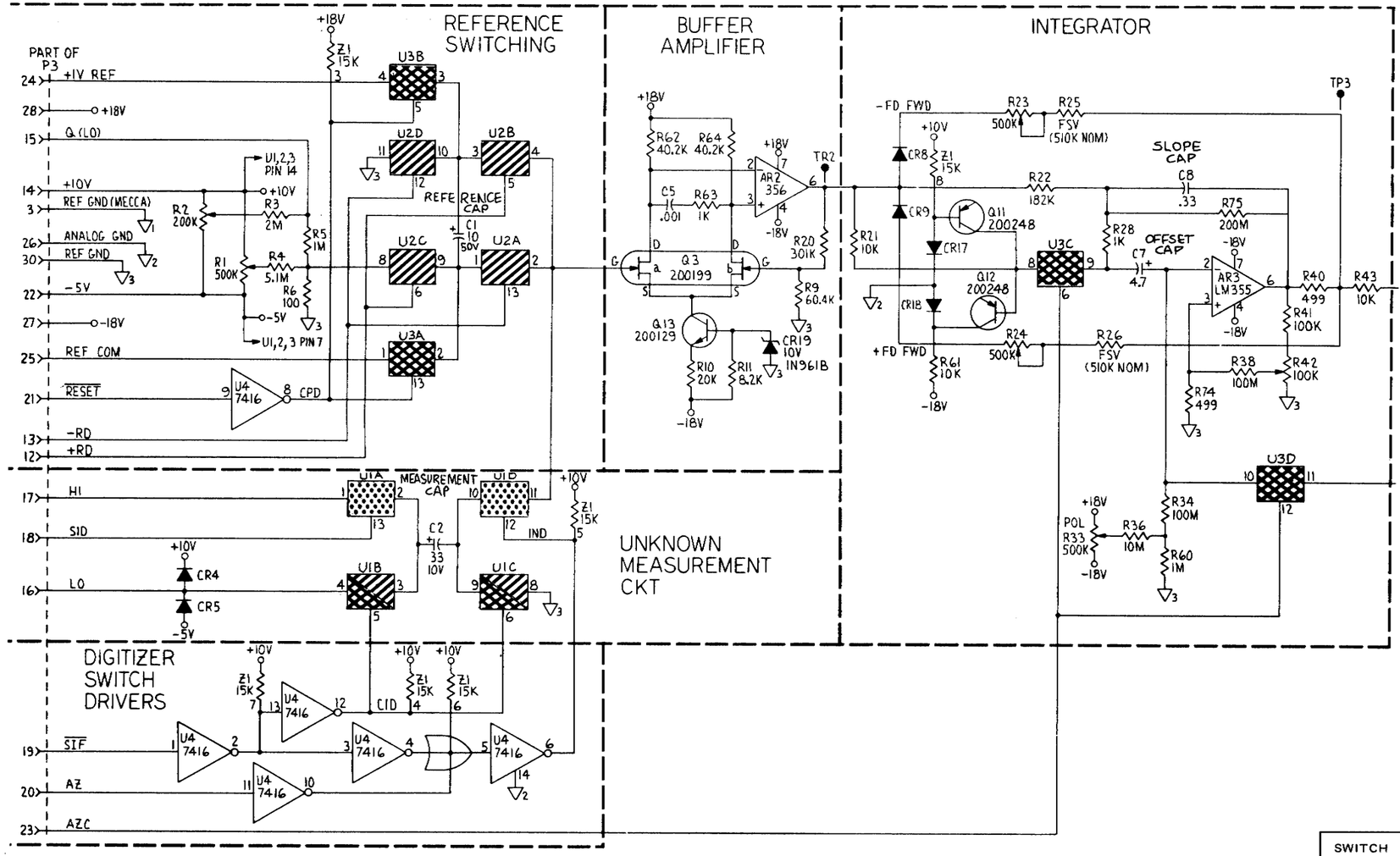
of drawing 432104, page 6-15. The circuit consists of an operational amplifier, a five-volt zener diode, driver transistor Q4 and protection diode, CR3. When supply voltages are applied to the circuit the overvoltage circuit rises to +10 volts. At this point the op-amp AR1 biases Q4 so that the collector remains at 10 volts. As current is drawn during a resistance measurement, the op-amp adjusts the bias so the output of Q4 remains at 10 volts under load. Thus the ohms reference voltage is held stable and the reference circuit is isolated from the ohms load. The overvoltage protection circuit is included to protect the instrument from accidental application of voltage while set for KΩ function.

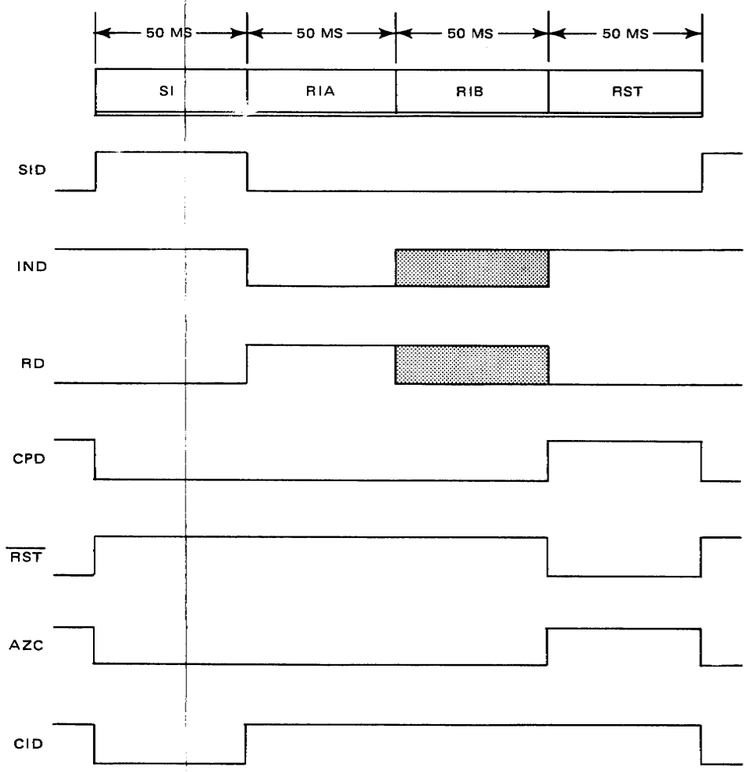
4.3.11 Open Input Terminal Clamp.

4.3.11.1 When there is no connection to the input terminals on the KΩ function the +10 volt reference line and reference common would tend to soar to the level of the power sources. To limit the drift Q9 and Q6 are biased to turn on and clamp these lines. This keeps the voltage on the test leads at a safe level and protects the components in a circuit under test.

4.3.12 Digitizer. .

4.3.12.1 The digitizer is the circuit which performs the analog-to-digital conversion of the measurement signal and is illustrated in figure 4.12. The digitizer uses the dual slope integration technique to perform the analog-to-digital conversion. Refer to figure 4.2 for the cycle timing relationships that relate to the dual slope integration. Refer to figure 4.13, page 4-11, for the reference and measurement input switching. Note that the switches are coded with cross-hatch shading. This illustrates the switch closure timing as shown in the timing chart at the right of figure 4.13. For example, U3A and U3B close to apply the +1 Volt reference voltage across the Reference Capacitor during the reset (RST) portion of the measurement cycle. During the reset portion of the measurement cycle the two reset switches close placing the offset capacitor across the output of the null detector amplifier. This charges the offset capacitor to a level equal to any offset voltage that appears at the output of the null detector amplifier. At the beginning of the signal integrate portion of the measurement cycle the reset switches (figure 4.13) open and the signal switch closes, thus placing the offset capacitor in series with the measurement signal from the isolator at the input of the integrator amplifier. Thus a positive or negative offset voltage is added to or subtracted from the signal being measured. The output of the integrator amplifier charges the slope capacitor for a fixed period of time (50 milliseconds). The charge placed on the capacitor is dependent on the magnitude or level of the measurement signal from the isolator. Refer to figure 4.2, note that there are two slopes shown representing the capacitor charging slope; these represent two measurement levels. Note that the time is the same for the charge for both measurements but that the charging rate and the final charge level is different. From this it can be seen that the signal integrate period is always the same length but the charging rate and level of the capacitor varies with the measurement signal. At the end of the signal integrate period the feed forward switch adds a small amount of charge to the capacitor to make up for a slight delay which is incorporated to allow similar lines and circuits to settle out between the reference integrate and signal integrate portions of the measurement cycle. This causes the slope capacitor charge voltage to increase slightly. At the beginning of the reference integrate period of the measurement cycle the signal switch opens and either the – reference switch or the + reference switch closes to apply a reference voltage to the input of the integrator amplifier opposite in polarity to the voltage of the measurement signal previously applied. This reference voltage is applied to the integrator amplifier and causes the slope capacitor to discharge at a fixed rate. When the slope capacitor reaches the zero level the null detector amplifier produces a null detect pulse. Note that in figure 4.2 that for both measurements the rate of discharge was the same, e.g., the slope is the same angle. Also note that for different measurement signals input the zero crossing occurs at a different point in time. Thus, it can be seen that the time





SWITCH					
U1-13	SID	▒	▒			
U1-12	IND	▒	▒			
U2-5/6	+ RD			▒	▒	
U2-12/13	– RD			▒	▒	
U3-5/13	CPD					▒
U3-6/12	AZC					▒
U1-5/6	CID			▒	▒	▒

Figure 4.13 - Integrator Input Switching

periods of the reference integrate portion of the measurement cycle is proportional to the value of the measurement signal. The output of the null detector is used by the Timing and Control circuits to stop the measurement counter. On figure 4.2 the Q_{e1} and Q_{e2} signals shown are timing signals generated by the measurement counter chip and used by the Timing and Control circuits for circuit synchronization and generation of control signals.

4.3.12.2 INTEGRATOR INPUT SWITCHING.

4.3.12.2.1 The A-to-D process called integration requires that the measurement signal from the isolator output, which has been conditioned (filtered, amplified, or attenuated), to be applied to the input of the integrator, whose R/C components allow the output to charge at a linear rate for 50 msec, called signal integration. The process now disconnects the measurement signal and applies a stable reference voltage opposite in polarity (of the measurement signal) to return the integrator output back to a zero voltage, to be sensed by the null detector as "zero crossing," called reference integration. The reference integration period is approximately 50 μsec for zero input signal, 50 ms for full scale signals (100,000 counts) and 100 msec for full scale + 100% overrange signals (199,999 counts). A period of 50 msec follows the reference integration period called "reset." During the Reset period, the +1V Reference Voltage from the Reference Generator is applied to a 10 μF/50V capacitor (C1) by COS/MOS bilateral switches to store the Ref +1V until use during the reference integration period. The drive signal for this sequence is called CPD or inverted $\overline{\text{Reset}}$ from the Timing and Control circuitry on the main PCB.

At the start of the Reference integration period, the Voltage stored on C1 must be applied to the integrator. If the measurement signal were plus, a –1 volt Reference must be used to complete the integration sequence. This is accomplished by use of COS/MOS bilateral switch configurations that reference C1 "+" to (Mecca) ground and connect C1 "–" to the integrator input. The drive signal required during the reference integrate sequence is "–" RD from the Timing and Control logic circuits on the main PCB, which was established by the polarity detection circuits during the start of signal integration.

Measuring a negative signal requires that a positive reference voltage be configured during reference integration by a drive signal called "+" RD.

The capacitor is used to store a voltage potential at Reset to be used, either positively or negatively, during the following reference integrate period. The "store" to "use" period, signal integrate, is 50 msec which, because of the high COS/MOS "OFF" resistance, does not "load" and/or derate the voltage on the capacitor. Following the reference integrate period is Reset which will again "charges" or "refills" the capacitor should any de-rating of the reference +1V occur.

The measurement signal, from the isolator output, is coupled to the integrator input through a configuration of COS/MOS bilateral switches and a measurement capacitor, C2. During the reset period, before signal integrate, the input to the integrator and C2 "–" are connected to (Mecca) ground while C2 "+" is connected to isolator "low" which removes any residual charge on the measurement cap. At the start of signal integration, C2 "–" is released from (Mecca) ground; C2 "+" is released from isolator output low and switched to isolator output high that places a measurement voltage on the integrator input to start a positive or negative output slope for the next 50 msec.

4.3.12.3 BUFFER AMPLIFIER.

4.3.12.3.1 The maximum measurement signal that can be resolved is ±2 volts while the reference voltage is ±1 volt. For the integrator to perform properly, a higher voltage is required by the integrator circuit to produce a slope with more velocity to prevent false triggering (at low level signals) and provide a more defined reference slope to detect zero or null. An amplifier with a gain factor of 5 is used to interface the input switching circuits and the actual integration amplifier circuit. With the gain as a constant, it applies to both the measurement signal for the signal integrate period and for the reference voltage during the reference integration sequence. It consists of a discrete dual FET input stage with a constant current generator, an operational amplifier, and the resistor values to achieve the required gain (x5).

4.3.13 Timing & Control Circuit.

4.3.13.1 Operation of the 5100AF is controlled by the Timing and Control circuits (figure 4.14, block diagram). These circuits provide synchronization and control signals which control the sequence of operation referred to as the measurement cycle. Figure 4.2 illustrates the measurement cycle timing. Note that the timing waveforms in the upper portion of the figure illustrate timing and polarities for a positive measurement signal while the lower portion illustrates the negative input example.

The differences between the upper and lower portions of the figure are the polarity of the input signal, the integrator slope and polarity, the timing of signal switch, reference switch and reset switch. The following description of the operation of the timing and control circuits refers to the simplified block diagram (figure 4.14) and the timing chart (figure 4.2).

Four timing events are established by the CMOS chip, 3814 counter, U10 on the main PCB. Since the 3814 counter only has the capability of resolving a 4-1/2 display an additional counter is used between the clock circuit and the 3814 counter to provide the least significant digit (LSD) for a total of 5-1/2 full digits on the readout PCB. An internal clock frequency of 2 MHz drives the LSD counter, whose output of 200 kHz is fed to the 3814 counter. The

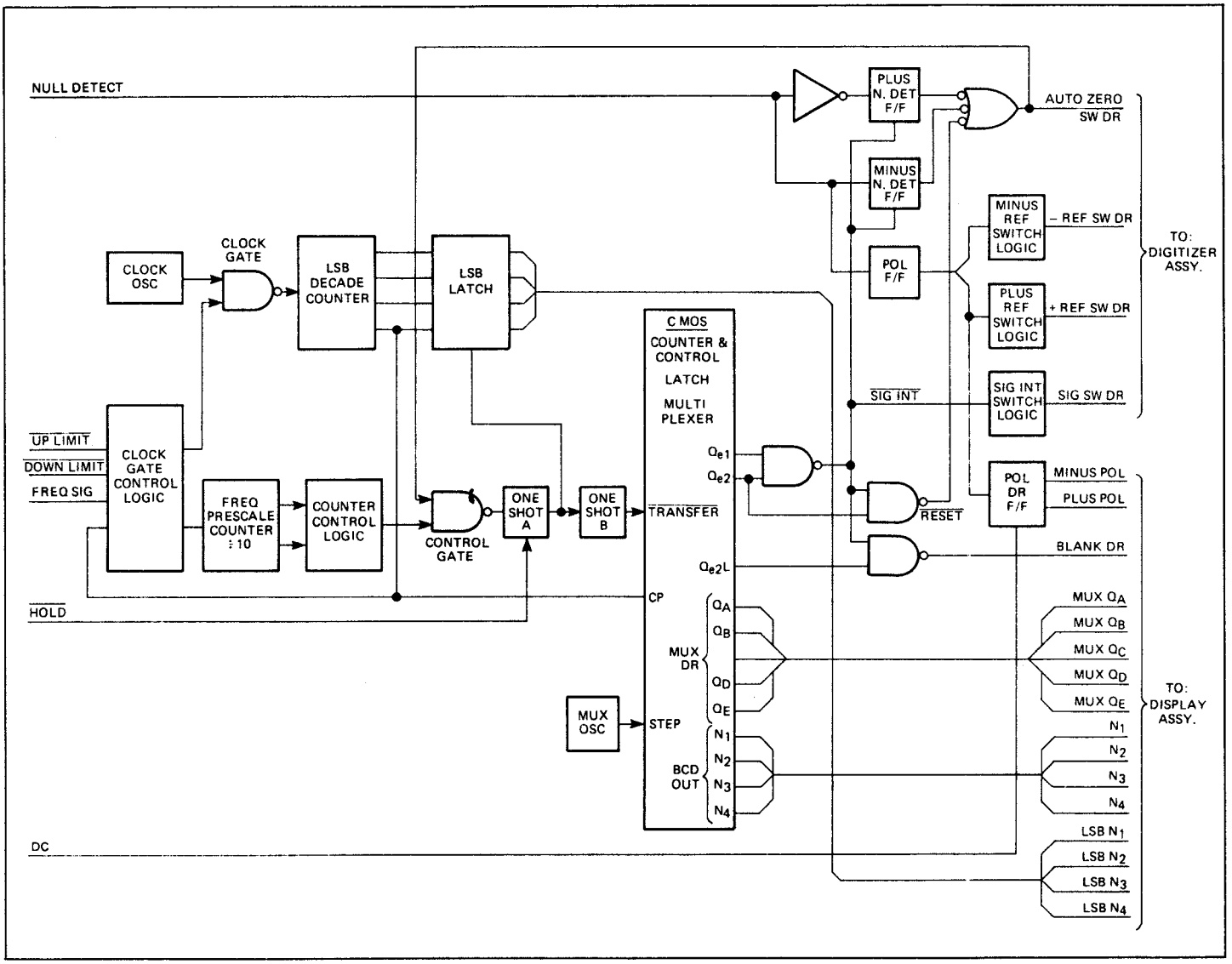


Figure 4.14 - Timing and Control

3814's 1/2 digit counter has two outputs, Q_{e1} and Q_{e2}, that establish four timing events of 50 msec each that will be used to convert (digitize) an analog expression into its digital equivalent. The timing sequences are as follows:

$Q_{e1} = 1, Q_{e2} = 1$
50 msec, counts from 300,000 to 399,999 called $\overline{\text{Signal Integrate}}$

$Q_{e1} = 0, Q_{e2} = 0$
50 msec, counts from 000,000 to 099,999 called Reference Integrate. This count total is referred to as full scale

$Q_{e1} = 1, Q_{e2} = 0$
50 msec, counts from 100,000 to 199,999 also called Reference Integrate. This count total is referred to as full scale plus 100% over-range

$Q_{e1} = 0, Q_{e2} = 1$
50 msec, counts from 200,000 to 299,999 called reset (FIXED)

In the following example a +1.0V DC input signal is applied to the isolator amplifier input. The isolator, at a gain of 1, has an output of +1.0V DC. When the signal integrate period is detected, this +1.0V DC is coupled to the Buffer/ Integrator by the configuration of the bilateral switches and measurement cap of the input switching circuit resulting in a negative going slope at the integrator output of approximately –5.0V at the end of the 50 msec period. The null detector senses the negative slope voltage and causes its output to go to a positive TTL level to be applied to U16-2, the D input of the polarity F/F. This causes U16-5, the Q output to be logic high, which when applied to the D input of the Polarity Drive F/F, U16-12, causes the $\overline{Q}$ output, U16-8 to be logic low to annunciate the "plus" symbol on the readout.

At the start of the signal integrate period, the outputs of U13-6 and U6-12, $\overline{\text{Signal Integrate}}$, go logic low. The low level of U6-12 is applied to the "clear" inputs, pin 1 and 13 of U15, that cause the $\overline{Q}$ outputs, pin 6 and 8, to go logic high to be applied to U14, pins 1 and 2 respectively. $\overline{\text{Signal Integrate}}$ at a logic low causes the output of U13-11, $\overline{\text{Reset}}$, to go logic high, which is also applied to U14 at pin 13, which results in the output U14-12 to be logic low called "internal reset" or auto zero (AZ). The counter control F/F $\overline{Q}$ output of U9-6 goes logic high at the start of reference integration, arming the input to the gate at U8-5. When the null detector senses zero, "internal reset" will go logic high at U8-4, causing a falling edge at U8-6 to trigger one-shot A to transfer the BCD count in the LSD counter, U3, into the LSD latch, U7. The $\overline{Q}$ output of one-shot A, U11-4, triggers one-shot B, causing a negative pulse (40 μsec) at U10-2, $\overline{\text{Transfer}}$ for the 3814, which stores the BCD count in the 4-1/2 decade counters into the latches to be multiplexed and decoded for the seven-segment display LEDs.

The internal reset (AZ) that goes low at the beginning of signal integration, is inverted twice through U5 and U18, called AZC, and used in the integrator to disable U3C and U3D bilateral switches from a reset state called "Auto Zero."

The $\overline{\text{Signal Integrate}}$ output from U13-6 is inverted at U13-3 and applied to U19-12 where the output at pin 11 is inverted, designated $\overline{\text{SIF}}$ on the digitizer PCB, after three inversions through U4 to become the IND drive signal for U1D. The $\overline{\text{SIF}}$ on the main PCB at U19-11 is inverted through U18-2 to drive bilateral switch U1A which, with bilateral switch U1D couple the isolator output voltage to the buffer/integrator during the signal integrate period. Pin 13 of U19 on the main PCB, labeled $\overline{\text{FQ}}$, is an inactive control line from S4 (disabled) always at a logic high; thus, in effect, making U19 from pin 12 to 11 an inverter with a positive input.

During signal integration U17-12, internal reset, (AZ) is logic low and U17-11, signal integrate, is logic high causing the output, U17-13 to be logic low. At the beginning of signal integration, it was established that the polarity was positive as a result of the logic high at the polarity F/F, U16-5, coupled to U19-9 to enable the NAND gate input. The logic high at the output of U19-8 is inverted through U18 and becomes logic low at pin 6.

All functions of signal integration have now been accomplished. The measurement signal from the isolator output has been coupled to the buffer/integrator input. The integrator has been released from Auto Zero by the switches and the output is moving at a negative slope and polarity has been sensed and annunciated.

At the end of signal integration, the CMOS counter is reset to zero. The output of U19-11 goes to logic high and U18-2 goes logic low disconnecting the measurement signal from the buffer/integrator input. Signal integrate at U17-11 goes logic low, causing the output at U17-13 to go logic high enabling U19-10. The low output of U19-8 is inverted to a logic high, designated – RD, to drive the logic switching circuitry on the digitizer PCB to configure the reference capacitor using U2A and U2D bilateral switches to apply a −1V to the buffer/integrator input. The CMOS counter will reset to zero again after the first 10 counts (100 counts for the LSD counter) or approximately 50 μsec. This is used to "mask" the switching transients during the transition from signal integrate to reference integrate, which is known as "delayed dual slope." The susceptibility to false triggering during signal to reference integration is much greater with signal inputs at or near zero. The feed forward (+ and –) circuit in the integrator compensates for the delay caused by the CMOS counter 10 count reset as the integrator output ramps back toward zero; hence, null detect.

When zero is detected by the null detector for the +1V signal, the output is a negative going pulse of 1.6 msec duration. When applied through U6 inverter to the clock input of the + ND F/F, U15-3, the $\overline{Q}$ output at pin 6 goes logic low. This causes the internal reset (AZ) line at U14-12 to go high which disconnects the −1V reference voltage from the buffer/integrator input, configures the integrator to the condition called "Auto Zero," and triggers the one-shots (A and B) to transfer the BCD value of the LSD and CMOS counters into their respective latches to be coded (seven segment), multiplexed, and displayed.

The digitizing sequences used thus far, signal and reference integrate (full scale), have only taken 100 msec. The remaining sequences, reference integrate (overrange) and "fixed" reset, will account for the other 100 msec. The overrange reference integrate sequence will be an internal reset time as null detect has taken place. When the "fixed" reset period is initiated, caused by a logic low at the output of U13-11, $\overline{\text{Reset}}$ is inverted on the digitizer PCB, labeled "CPD," and drives the bilateral switches U3 A and B to "refill" the Reference Capacitor from the +1V output of the Reference Generator.

If a null detect is sensed, during reference integrate, sequence state 2, before 10,000 counts (10% of range) and the DMM is not on the lowest range (in auto range) a "Down Range" is commanded.

Table 4.1 - Sequence Chart

+ Signal = 1.0000V DC, 1 Range

Q_{e1} = High, Q_{e2} = High	(1)	$\overline{\text{SIG INT}}$ goes low
	(2)	+ N.D. F/F (U15) $\overline{Q}$ goes high
	(3)	– N.D. F/F (U15) $\overline{Q}$ goes high
	(4)	$\overline{\text{RESET}}$ goes high
	(5)	INTERNAL RESET goes low (caused by 2, 3, 4)
	(6)	ONE-SHOTS (Armed for digitizing sequence)
	(7)	RESET SW goes low (releases sw's from Auto Zero)
	(8)	SIG SW goes high (connects iso out to integrator in)
	(9)	NULL DETECTOR OUTPUT goes high (to detect polarity)
	(10)	POL F/F Q OUTPUT goes high (to enable – ref sw @ ref int) and (set pol dr F/F Q output low)
Q_{e1} = Low, Q_{e2} = Low	(1)	$\overline{\text{SIG INT}}$ goes high
	(2)	SIG SW goes low (disconnects iso out from integrator in)
	(3)	– REF SW goes high (connects –1V ref to integrator in)
Q_{e1} = High, Q_{e2} = Low	(1)	NULL DETECTOR OUTPUT goes low pulse (zero detect)
	(2)	+ N.D. F/F (U15) $\overline{Q}$ goes low (causes internal reset to go high)
	(3)	INTERNAL RESET goes high (causes one-shots to go low pulse)
	(4)	ONE-SHOTS pulse low (signals LSD & CMOS counter to stop count)
	(5)	– REF SW goes low (disconnects –1V ref from integrator in)
	(6)	RESET SW goes high (closes reset switches – Auto Zero)
Q_{e1} = Low, Q_{e2} = High	(1)	RESET SW is high (Auto Zero)
	(2)	$\overline{\text{RESET}}$ goes low (CPD refills ref cap)

If a null detect is not sensed before 199,999 counts is accumulated in the LSD and CMOS counter, an "overload" is annunciated on the readout by a flashing 200000 at the read rate for a manual range or highest range per function. If the DMM is in auto range and overload is sensed, the range counter, U20, is advanced one range. This is a result of the Q_{e2} output of the CMOS 3814 counter, which is latched as an output called Q_{e2}L or O/L. When null detect has not been sensed when the 4th sequence (fixed reset) is entered, the Q_{e2}L (O/L) output of U10-9 goes logic high to detect "overload" or "uprange."

If the input signal to the DMM is of negative polarity, the null detector output is applied to U16-2 of the polarity detect F/F, which is a logic low during signal integration. This causes the polarity F/F Q output at pin 5 to be applied to the D input of the Polarity Drive F/F, U16-12, to cause the Q output at pin 9 to go logic low and annunciate the minus polarity symbol on the display. The $\overline{Q}$ output of the polarity detect F/F, U16-6, goes logic high and enables the circuitry for the + RD (plus reference drive) when the reference integrate sequence is started. This causes the bilateral switches, U2 B and C, on the digitizer PCB to configure the charge on the reference cap so that a +1V is applied to the buffer/integrator input.

The null detector output, for a negative input signal, goes logic high at the end of reference integrate (zero detect) and is applied to the "clock" input of the – ND F/F, U15-11, and causes the $\overline{Q}$ output at pin 8 to go logic low at null detect to terminate the LSD and CMOS count.

In addition to the illustrations, a sequence chart is presented in table 4.1. This chart is a synopsis of the sequence of operation of the timing and control circuits for one measurement cycle. Its basic purpose is for reference after reading the detailed description presented in the following paragraphs. It will also serve as a handy reference to use while reading the detailed description.

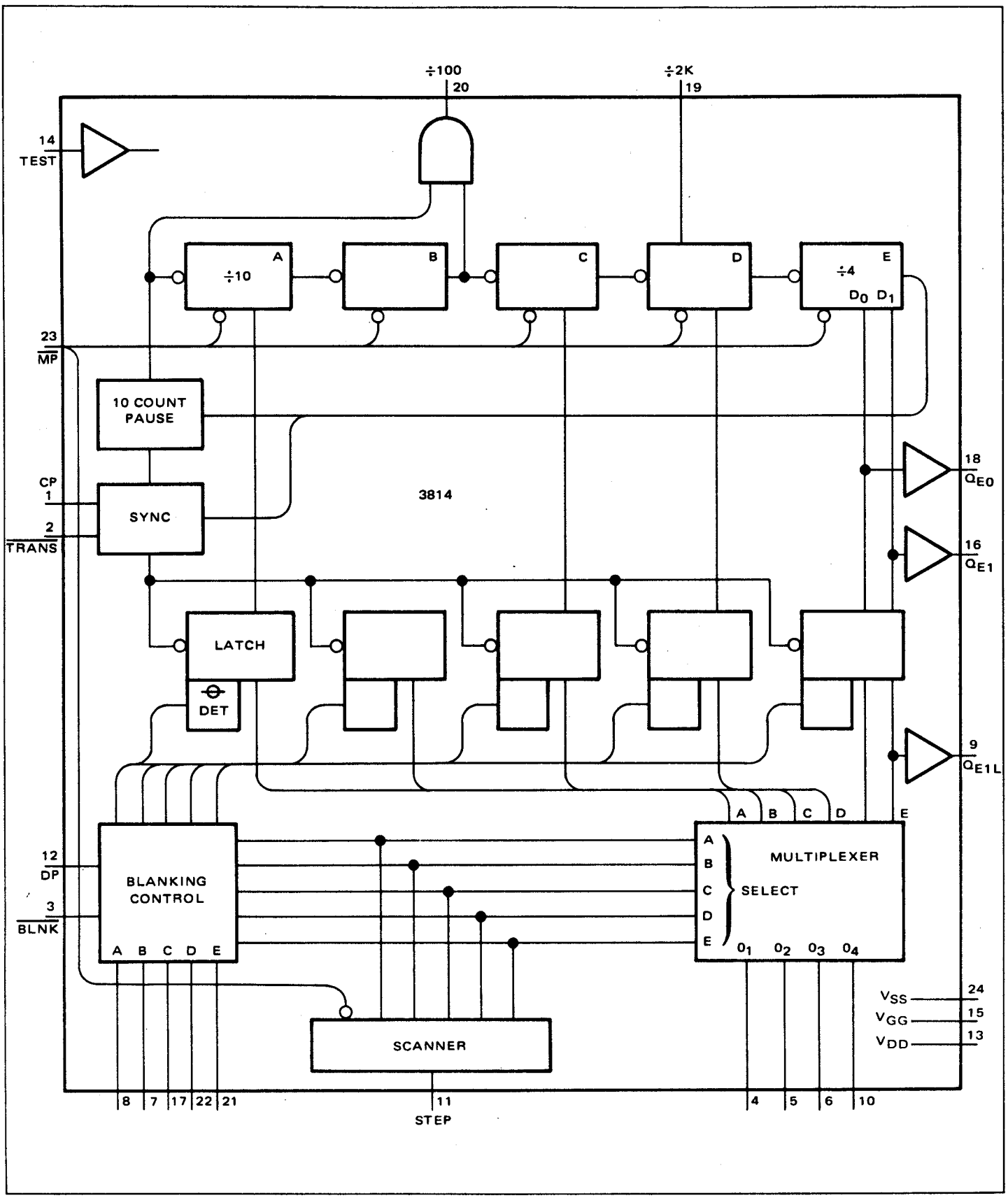


Figure 4.15 - Logic Array

4.3.14 Large Scale Integration Logic Array (Counter).

4.3.14.1 The heart of the instrument is the 3814 Digital Voltmeter logic array, shown on figure 4.1 as the counter, latch, 4-line decoder, and multiplexer. A more detailed illustration of this device is shown in figure 4.15. It contains four full decade counters, two overflow latches, an underrange output, an overrange output, outputs to drive a BCD to seven segment converter, and decoded outputs to strobe the display. The 3814 counts four full digits and the overrange digit. The output of the LSD decade counter is 200 kHz which drives the CP input to the 3814 chip. The decade counters change state on the rising edge of the clock pulse.

4.3.14.2 A MUX oscillator is used to drive the step input to the 3814. The frequency of the output at U1-4 is 500 Hz ±10%. The step input clocks a ring counter that drives the multiplexer.

4.3.14.3 The 1 output of the fourth decade counter in the 3814 is buffered and used as a divide-by-two thousand (÷2,000) output. This output is used to indicate a signal that is less than 10% of full scale. If the transfer pulse is enabled before the divide-by-2,000 output goes high the output will signal the auto range circuitry that a down range change must be made.

4.3.14.4 The Q0 and Q1 flip-flop outputs of the 5th counter are designated as Q_{e1} and Q_{e2} outputs. These outputs step the DMM through the various periods of the integration process. The signal codes are:

Q_{e1}	Q_{e2}	
1	1	50 ms – Signal integration – decade counts from 300,000 to 399,999
0	0	50 ms – Reference integration – decade counts from 000,000 to 099,999 (F/S)
1	0	50 ms – Reference integration – decade counts from 100,000 to 199,999 (F/S +100%)
0	1	50 ms – Reset – decade counts from 200,000 to 299,999

4.3.14.5 The Q_{e2} output is latched and used as the $Q_{e2}L$ output. If a DMM has a full scale + 100% count of 199,999 using the 3814, the high state of $Q_{e2}L$ is used to indicate an overrange condition. The $Q_{e2}L$ output causes the display to read 200,000 at a flashing rate.

4.3.14.6 The edge sensitive transfer input causes the BCD data in the counters to be stored in the latches on the falling edge. Synchronization with the clock is necessary to prevent loading and storing erroneous counter states at a "carry" is trickling through the counters. A transfer command is accepted once during an integration cycle. An internal flip-flop is reset by the counter transition from 399,999 to 000,000. It is set when a transfer occurs and remains set until the next integration sequence. No transfers will be accepted when this flip-flop is set.

4.3.14.7 The clock pulse is constantly adding counts to the counter. As previously mentioned the states of Q_{e1} and Q_{e2} control the state of events that take place during an integration sequence.

4.3.14.8 $Q_{e1} = 1$ and $Q_{e2} = 1$. The counter advances from 300,000 to 399,999. This is the signal integration period. At this time the DMM input signal which has been attenuated, amplified, converted, and/or filtered and connected to the integrator input through a bilateral switch and measurement cap. The feed forward circuit of the integrator adds 10 digits of voltage to the integrator output to mask the switching transients that occur during the transitions from signal integrate to reference integrate.

4.3.14.9 $Q_{e1} = 0$ and $Q_{e2} = 0$. During this period the signal switch is turned off and a reference (plus or minus) is connected to the input of the integrator through bilateral switches and reference cap. The decade counter is set to 000,000 and the 3814 will ignore the next 10 counts. Because of the 3814, the first 10 counts are ignored. This period allows for masking the noise at the time when the signal integration is switched to the reference integration to prevent false zero detection at or near zero analog input signals. The count is started from 000,000 until the null detector crosses zero and signals the end of the reference integration period. Zero detect signals the transfer input to store the BCD count of the decade counters into the latches. If the transfer occurs before the ÷2000 output goes true, the signal is less than 10% of full scale and a down range is commanded if the DMM is in auto range.

4.3.14.10 $Q_{e1} = 1$ and $Q_{e2} = 0$. This reference integration period is from 100,000 to 199,999 which is the F/S + 100% capability of the DMM.

4.3.14.11 $Q_{e1} = 0$ and $Q_{e2} = 1$. This is the reset period when the analog and reference inputs to the integrator are removed and bilateral switches short the integrator input to

the output in a configuration called auto zero. The count of this period is from 200,000 to 299,999. If the $Q_{e2}L$ output goes true before zero detect signals a transfer, an uprange is commanded if the DMM is in auto range and/or overload is detected and the display indicates overrange.

4.3.14.12 The step input from the MUX oscillator output presents the multiplexed BCD outputs capable of driving a single decoder/driver, such as a SN7447. The decoded outputs 0_a to 0_e drive transistor circuitry that strobes the anodes of the display devices one at a time.

4.3.15 4-to-7 Line Decoder.

4.3.15.1 The 4-to-7 line decoder is shown on figure 4.16. This device is simply a matrix decoder that converts BCD code to 7-line code for display purposes. It's driven by the BCD code from the 3814 counter chip and its 7-line output is tied in parallel to all of the display LEDs.

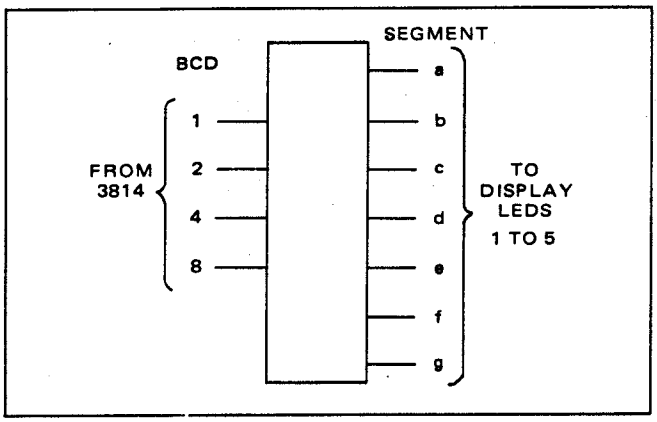


Figure 4.16 - 4-to-7 Line Decoder

4.3.16 BCD to Decimal Decoder.

4.3.16.1 The BCD to Decimal converter shown in figure 4.17 uses the range information from the range circuits to control the position of the decimal point on the display. This device is simply a 3-line to 7-line converter. The range code input determines which decimal point is lit.

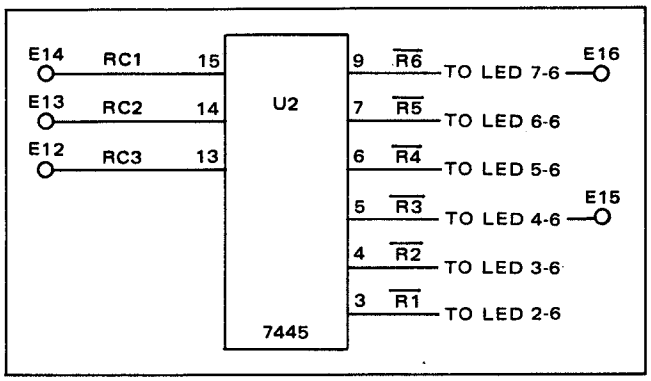


Figure 4.17 - BCD to Decimal Decoder

4.3.17 LED Display.

4.3.17.1 A functional diagram of the display circuit is shown on figure 4.18. The display consists of six 7-bar LED display devices and the polarity display device. The output of the 7-segment decoder is tied in parallel to the inputs of the five 7-line display devices. When the digit code and 7-bar form is on the line for the low order digit display device the multiplexer in the counter chip will energize the enable line A and the device will display the numeric value on the 7-line bus at that time.

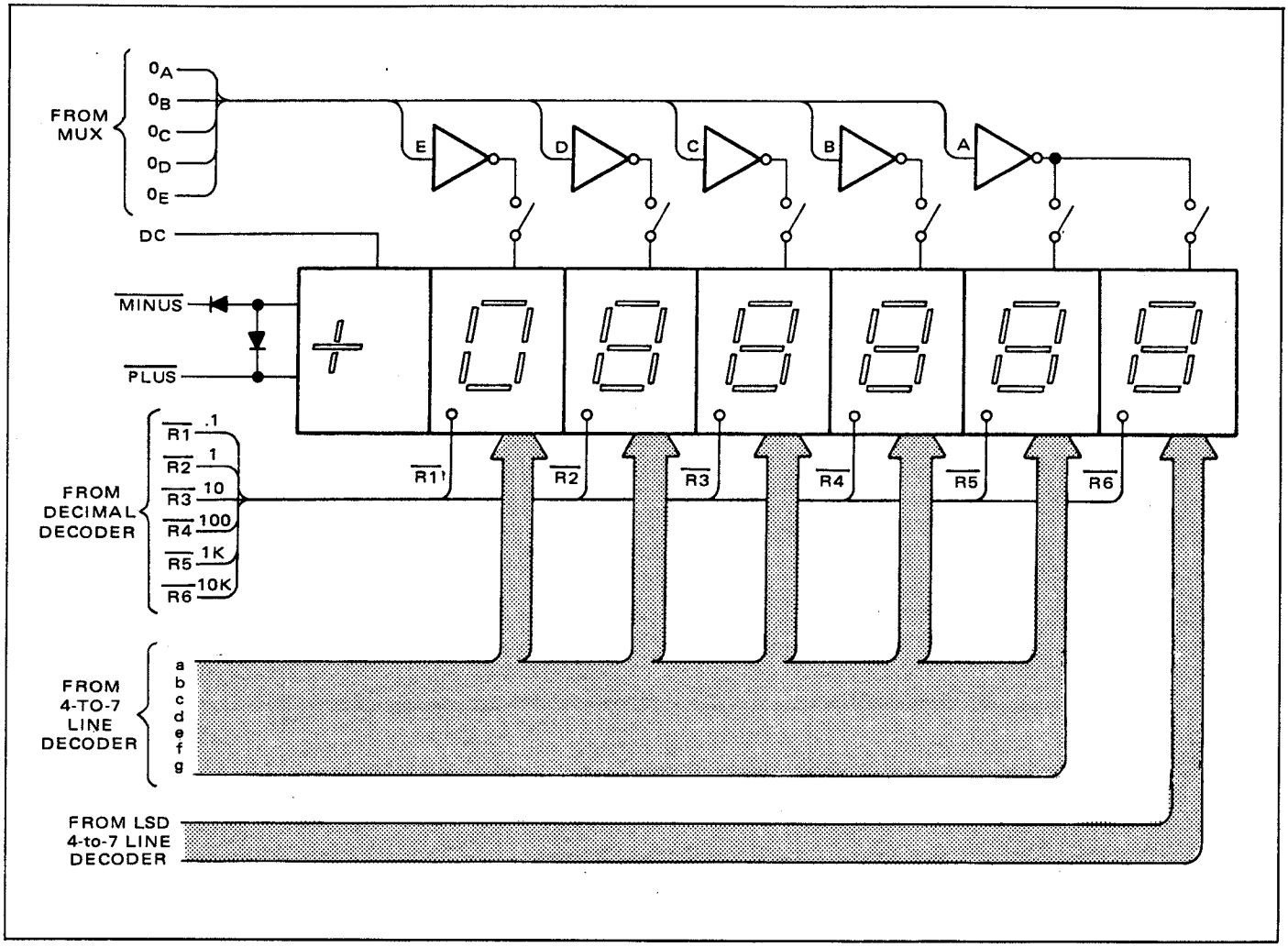


Figure 4.18 - LED Display

SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.1.1 This section contains information necessary to check the calibration of the Model 5100AF, perform calibration adjustments and to troubleshoot the instrument in case of malfunction. The calibration checks are also used for receiving inspection or specification validation purposes. This maintenance information is organized to provide for two levels of maintenance.

5.1.2 The section is divided into three major subsections; (1) Calibration Checks, (2) Calibration Adjustment and (3) Troubleshooting Performance Tests. The troubleshooting is further divided into Unit Performance Tests and Subassembly Performance Tests. The unit level performance tests are designed to check the instrument by function, such as AC Volts, and enable isolation of a malfunction to a replaceable module or subassembly. The subassembly performance tests are designed to check the operation of a module or subassembly and isolate a malfunction to an individual component or circuit.

5.2 CALIBRATION CHECKS.

5.2.1 This subsection of the Maintenance section contains instructions and reference information for checking the calibration of the Model 5100AF DMM. The instructions are presented in tabular form and are organized by instrument function. In addition, the test setup, input and control settings are provided for each step in the procedure. Test equipment required is listed in table 5.1.

Table 5.1 - Test Equipment Required for Calibration Checks and Adjustment

Function	Qty	Item	Minimum Use Specifications	Suggested Equipment
DC	(1)	Saturated Standard Cell Bank (6 cells)	1 ppm, certified	EPPLEY 106, GUIDELINE 9152/T6
	(2)	DC Calibrators	0.1 ppm resolution	FLUKE 332B, HP740B
	(1)	Fixed High Voltage Divider	1 ppm, certified	GUIDELINE 9700
	(1)	Voltage Divider Adjustable	0.1 ppm resolution	FLUKE 720A, JRL SVD-108
	(1)	Null Detector/μVoltmeters	1 μV sensitivity	FLUKE 845AR, HP419A
AC	(1)	Thermal Transfer Standard	35 ppm @ 400 Hz, 50 ppm @ 40 kHz	HOLT 6A
	(1)	AC Voltage Source	1 ppm resolution	HP745A/746A
Ω	(7)	Resistance Standards		
		100Ω	10 ppm	ESI SR1 with corrections
		1 KΩ	10 ppm	ESI SR1 with corrections
		10 KΩ	10 ppm	ESI SR1 with corrections
		100 KΩ	10 ppm	ESI SR1 with corrections
		1 MΩ	10 ppm	ESI SR1 with corrections
		10 MΩ	50 ppm	ESI SR1 with corrections
OTHER	(1)	Phillips head screwdriver #1	–	–
	(1)	Insulated Adjustment tool	–	JFD5284
	(1)	10 Kohm 1/4 Watt, 5% Carbon Resistor	5%	–
	(1)	1 Megohm 1/4 Watt, 5% Carbon Resistor	5%	–
	(2)	Minigator Clip Leads with Shields	–	–

Table 5.2 - DCV Calibration Check (6 Month, 20°C to 30°C Spec)

Input and Control Setting		
Function: DCV Range: .1, Manual Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper		Note: Offset greater than ±5 digits will require adjustment of R32 (front panel) on .1 range. Note: Guard (J105) must be strapped to SIG LO (J102).
Signal Range	Signal Input	Readout Performance Standard
.1 (manual)	.000000	±.000005
1 (manual)	.000000	±.000005
10 (manual)	.000000	±.000001
100 (manual)	.000000	±.000001
1000 (manual) (±1100 VDC Max.)	.000000	±.000001
Remove the jumper and apply the input voltages shown		
.1 (manual)	±.100000	±.099985 to ±.100015
1 (manual)	±1.00000	±0.99985 to ±1.00015
10 (manual)	±10.0000	±09.9985 to ±10.0015
100 (manual)	±100.000	±099.985 to ±100.015
1000 (manual) (±1100 VDC Max.)	±1000.00	±0999.85 to ±1000.15
Set DMM to Auto Range and apply the input voltage shown and verify that the instrument autoranges as shown		
±0099.99 VDC	DMM Down Ranges from	1000 Range to 100 Range
±009.999 VDC	DMM Down Ranges from	100 Range to 10 Range
±00.9999 VDC	DMM Down Ranges from	10 Range to 1 Range
±0.09999 VDC	DMM Down Ranges from	1 Range to .1 Range
±.200000 VDC	DMM Up Ranges from	.1 Range to 1 Range
±2.00000 VDC	DMM Up Ranges from	1 Range to 10 Range
±20.0000 VDC	DMM Up Ranges from	10 Range to 100 Range
±200.000 VDC	DMM Up Ranges from	100 Range to 1000 Range
Set voltage standard to 0V and remove input cables		

Table 5.3 - DC (3-Wire) Ratio X10 Calibration Check (6 Month, 0°C to 40°C Spec)

Input and Control Setting			
Function: DCV (S2) & Ratio (S5) Range: .1 (Auto) Input Terminals: J101 (Hi) and J102 (Lo) connected to signal (+ or –). J103 (Ext. Ref. Hi) and J104 (Ext. Ref. Lo) connected to +10 VDC			Note: Guard (J105) must be strapped to SIG LO (J102). Note: Shorting links used on the front panel input terminals must be disconnected.
Signal Range	Signal Input	External Reference Input	Readout Performance Standard
.1 (.01:1 Ratio)	±.100000 VDC	+10.000 VDC	±.099945 to ±.100055
.1 (.01:1 Ratio)	±.100000 VDC	+9.000 VDC	±.111050 to ±.111172
.1 (.01:1 Ratio)	±.100000 VDC	+8.000 VDC	±.124931 to ±.125069
.1 (.01:1 Ratio)	±.100000 VDC	+7.000 VDC	±.142779 to ±.142935
.1 (.01:1 Ratio)	±.100000 VDC	+6.000 VDC	±.166575 to ±.166757
.1 (.01:1 Ratio)	±.100000 VDC	+5.000 VDC	±.199889 to ±0.20038*
.1 (.01:1 Ratio)	±.100000 VDC	+4.000 VDC	±0.24952 to ±0.25048
.1 (.01:1 Ratio)	±.100000 VDC	+3.000 VDC	±0.33270 to ±0.33396
.1 (.01:1 Ratio)	±.100000 VDC	+2.000 VDC	±0.49905 to ±0.50095
*Note: Ratio X10 display greater than 200,000 counts requires manual uprange or autorange			
1. (.1:1 Ratio)	±1.00000 VDC	+10.000 VDC	±0.99945 to ±1.00055
10. (1:1 Ratio)	±10.0000 VDC	+10.000 VDC	±09.9945 to ±10.0055
100. (10:1 Ratio)	±100.000 VDC	+10.000 VDC	±099.945 to ±100.055
1000. (100:1 Ratio)	±1000.00 VDC	+10.000 VDC	±0999.45 to ±1000.55
Reduce signal voltage supply to 0 VDC and disable ratio switch, S5, to return DMM to DC function. Disconnect Ext. Ref. voltage from J103 and J104			
Note: 100:1 Ratio X10 with ±1000 VDC signal cannot resolve an Ext. Ref. voltage of less than +5 VDC, i.e., DMM will display overrange by a readout of 200000 flashing at the read rate.			
WARNING: The ratio technique used is 3-wire. When using a negative input signal, be careful to avoid ground loops and unreferenced power levels to prevent shock hazards to the operator and possible damage to associated test equipment.			

Table 5.4 - ACV (Averaging) Calibration Check (6 Month, 0°C to 40°C Spec)

Input and Control Setting			
Function: ACV Range: .1, Manual Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper			Note: Guard (J105) must be strapped to SIG LO (J102). Note: Signals below 0.1% of full scale are not specified.
Signal Range	Signal Input	Frequency	Readout Performance Standard
1 (manual)	.000000	N/A	0.00000 to 0.00060
10 (manual)	.000000	N/A	00.0000 to 00.0060
100 (manual)	.000000	N/A	000.000 to 000.060
1000 (manual)	.000000	N/A	0000.00 to 0000.60
Remove the jumper and apply the following input voltages (RMS, Sine)			
1 (manual)	1.00000 VAC	50 Hz to 20 kHz	0.99740 to 1.00260
10 (manual)	10.0000 VAC	50 Hz to 20 kHz	09.9740 to 10.0260
100 (manual)	100.000 VAC	50 Hz to 20 kHz	099.740 to 100.260
1000 (manual)	0500.00 VAC	50 Hz to 20 kHz	0998.40 to 1001.60
1000 (manual)	1000.00 VAC (max. input)	50 Hz to 20 kHz	0996.90 to 1003.10
Set Voltage Standard to 0V and remove input cables			

Table 5.5 - Kohms Calibration Check (6 Month, 0°C to 40°C Spec)

Input & Control Setting		
Function: KΩ Range: .1, Manual Input Terminals: J101 (Hi) and J103 (KΩ source) connected to J102 (Lo) and J104 (KΩ sink) with a copper jumper		Note: Guard (J105) must be strapped to SIG LO (J102).
Signal Range	Signal Input	Readout Performance Standard
All ranges	Short	.1 - .000020, 1 - 0.00020, 10 - 00.0020, 100 - 000.020, 1000 - 0000.20, 10,000 - 00002.0
Remove the jumper and apply the following resistance inputs		
.1 KΩ (manual)	100.000Ω	.099780 to .100220
1 KΩ (manual)	1.00000 KΩ	0.99780 to 1.00220
10 KΩ (manual)	10.0000 KΩ	09.9780 to 10.0220
100 KΩ (manual)	100.000 KΩ	099.780 to 100.220
1000 KΩ (manual)	1.00000 MΩ	0997.80 to 1002.20
10000 KΩ (manual)	10.0000 MΩ	09978.0 to 10022.0
Auto	Short	Auto Ranges to .1 KΩ Range
Auto	Open	Auto Ranges to 10 MΩ Range, flashing 20000 (O/L)@ read rate
Remove resistance standards and input cables		

5.3 CALIBRATION ADJUSTMENTS.

5.3.1 Test setup and adjustment instructions are presented in this subsection. If performance of the calibration checks indicate the need for adjustment, perform the appropriate adjustment procedure. Like the calibration checks the adjustment procedures are organized by instrument function. This section covers the calibration of the Dana Model 5100AF Digital Multimeter and is designed to return the instrument to its published specification for indefinite periods of time. The procedure consists of applying known input levels and adjusting the appropriate component for the indicated value. A list of equipment required to perform the calibration procedure is provided in table 5.1.

5.3.2 Disassembly of the instrument case is as follows:

a. Place instrument on a flat level surface with the bail extended towards the back of the instrument.

b. Disconnect the power cable and remove the screws (see table 3.2) on the back panel.

c. Slide the instrument out of the case.

5.3.3 The following steps are performed prior to making any adjustments to the instrument.

a. Check the line voltage requirements stamped on the serial tag located on the back of the instrument and insure that the available power source is the same. Connect the instrument to the line and set the power switch to ON. Allow at least 30 minutes for the instrument to temperature stabilize.

b. Refer to the operating manuals provided with the test equipment to be used and provide appropriate warmup time.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

5.3.4 DC Voltage Sources.

5.3.4.1 Calibration of the 5100AF to its published specifications requires the use of metrology standards and techniques, which are presented in the following paragraphs.

5.3.4.2 The 10V, 100V, and 1000V range sources are derived by the method illustrated in figure 5.1. The setup is as follows:

a. Disconnect standard cell bank and μVmeter leads and set the DC calibrator on the desired voltage range of 10, 100, or 1000.

b. Adjust the decade voltage divider for a ratio equal to Voltage of the standard cells/Desired decade voltage.

c. Connect the μVmeter and adjust the DC calibrator source for the amount required to achieve null.

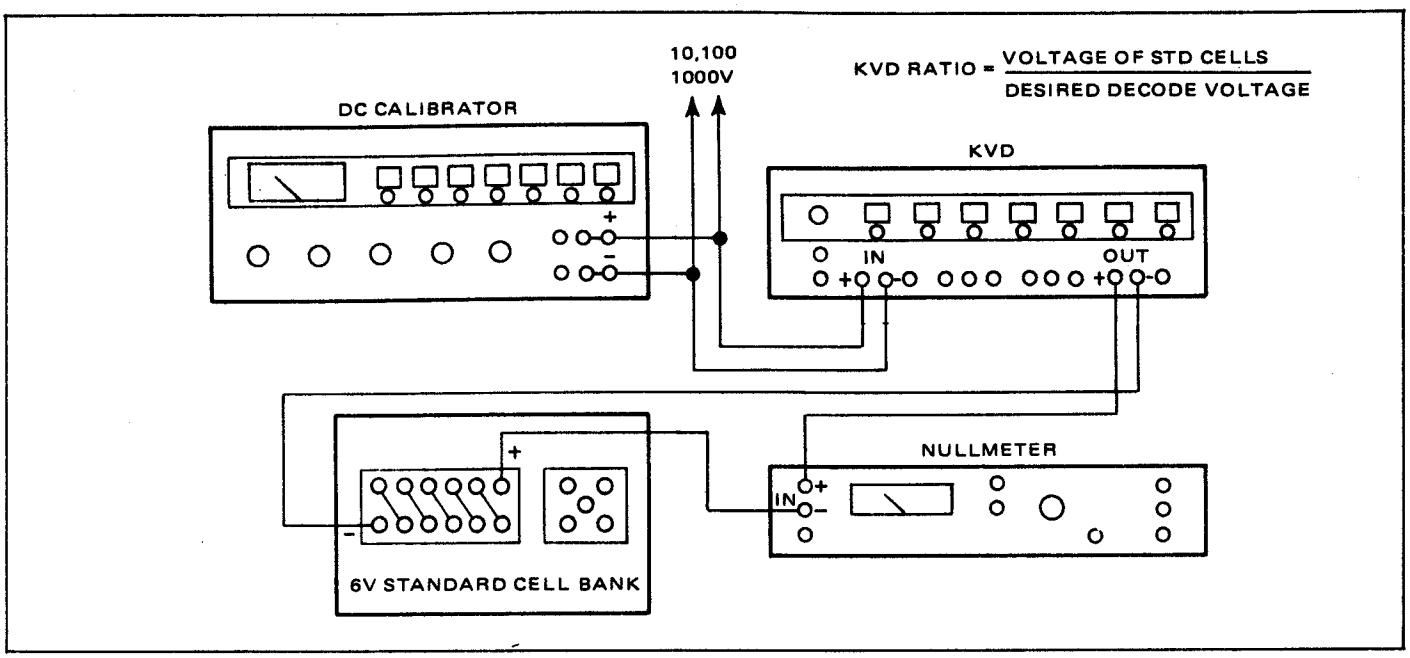


Figure 5.1 - 10V, 100V and 1000V Sources

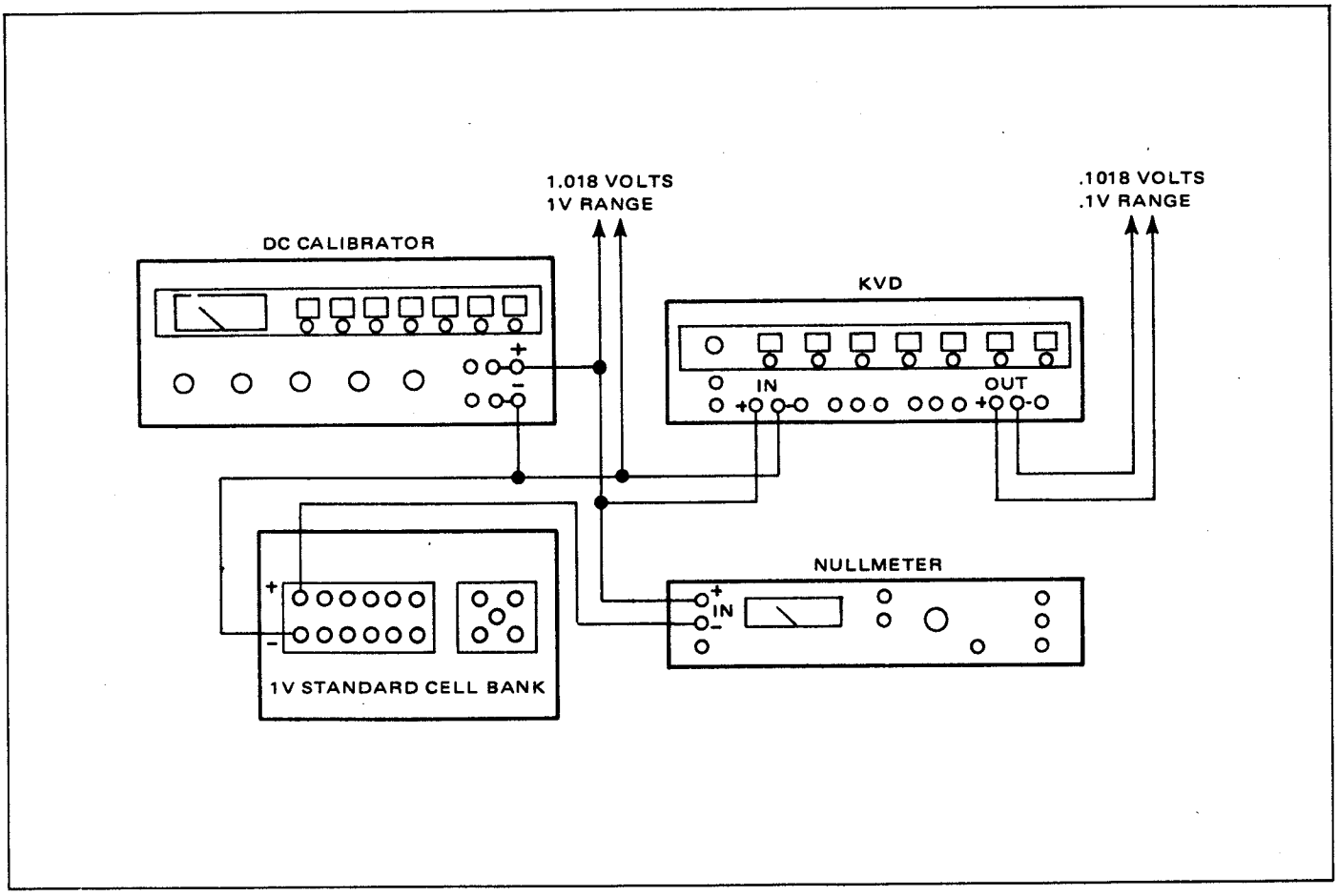


Figure 5.2 - 1V, .1V Sources

5.3.4.3 The 1 volt source is derived and equal in voltage to a single certified standard cell by the method illustrated in figure 5.2. The setup is as follows:

a. Disconnect the standard cell and μVmeter leads and set the DC calibrator for an output equal to the level of the certified cell.

b. Connect the μVmeter and adjust the DC calibrator source for the amount required to achieve null.

5.3.4.4 The .1 volt source is derived from the 1 volt source by use of a precision voltage divider in the method illustrated in figure 5.2.

5.3.4.5 The divider is set to .1000000. The output of the divider is then a precise 1/10th of the 1 volt input and is used to calibrate the .1 DCV range of the DMM.

5.3.5 AC Voltage Source (Sinusoidal RMS).

5.3.5.1 The generation of accurate AC signals for calibrating the AC converter requires the use of a thermal transfer standard, a DC voltage standard, and a stable AC voltage source.

5.3.5.2 The test setup is shown in figure 5.3. Information on the use of the transfer standard can be obtained from the operator's manual.

5.3.5.3 The accuracy of the AC voltage source is equal to the sum of the transfer standard and DC voltage source accuracies.

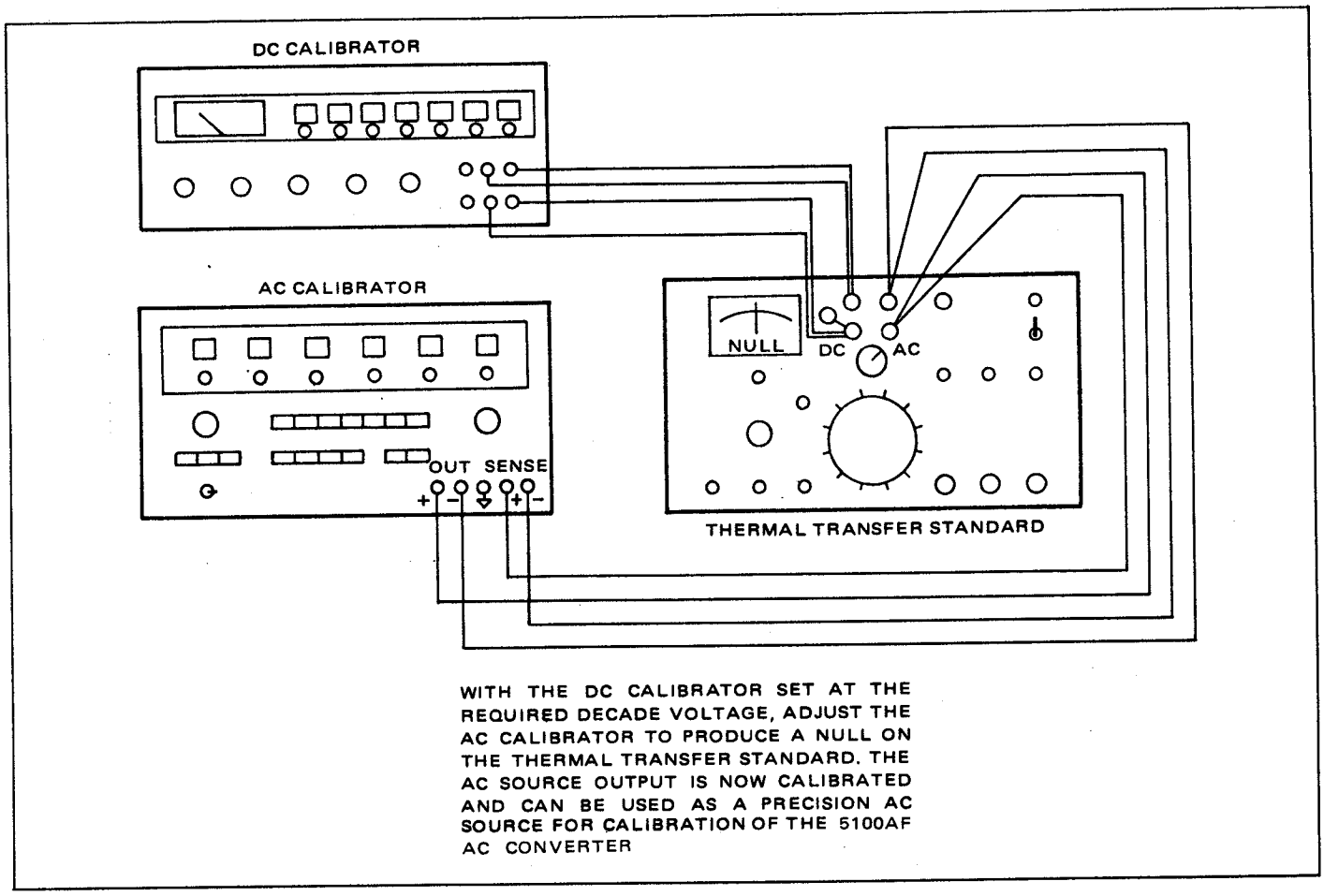


Figure 5.3 - AC Source

5.3.6 Familiarization.

5.3.6.1 Read all step-by-step procedures before starting calibration to verify that all required test equipment, tools, and miscellaneous hookup cables are available to perform the calibration procedure. Verify that all test equipment has been under power for the required amount of time prescribed by the manufacturer to attain full accuracy and/or stability.

5.3.7 Warmup.

5.3.7.1 Apply power to the 5100AF and allow 1/2 hour of warmup time.

5.3.8 Calibration Points.

5.3.8.1 Calibration points are shown in figure 5.4.

5.3.8.2 Access to the calibration points is by removal of the instrument case. This procedure is performed as follows:

a. Set DMM power switch to OFF.

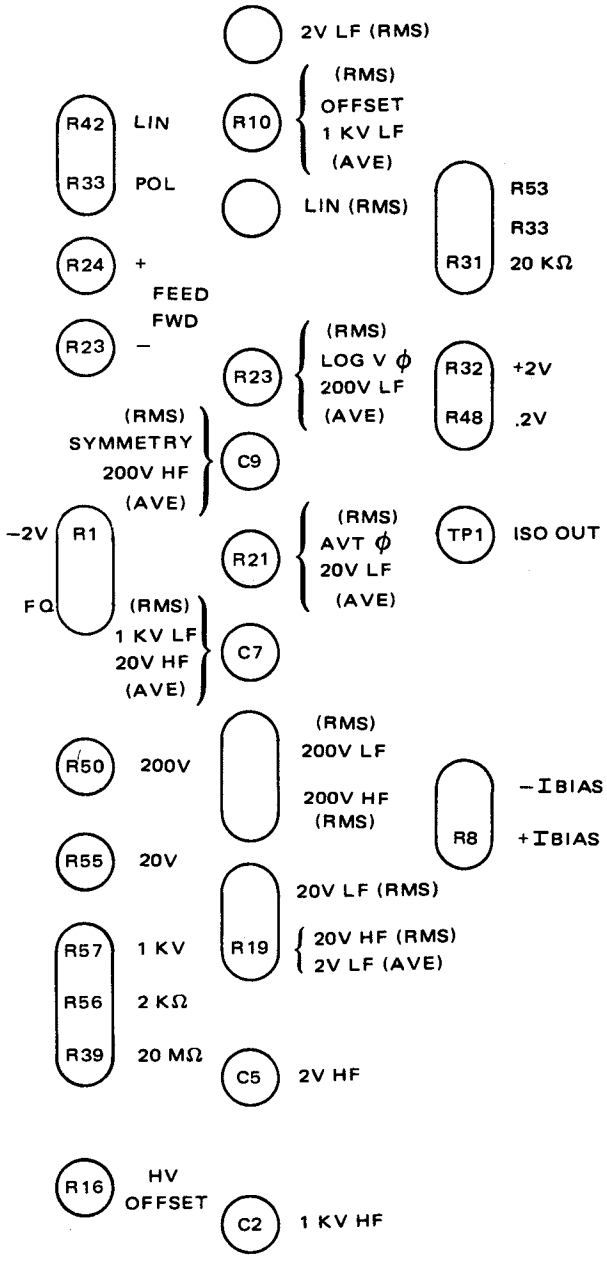
b. Remove line cord from DMM (J201).

c. Remove screws (2) from rear panel.

d. Slide DMM out of case.

e. Replace line cord to J201.

f. Set DMM power switch to ON.



DC CALIBRATION ⚠

(CONNECT MICROVOLTMETER TO ISO OUTPUT REF TO LO SENSE)

	INPUT	MODE	ADJUST
1.	SHORT	2V DC	FRONT PANEL "DC OFFSET"
2.	1 MΩ	2V DC	+IBIAS
	(REPEAT 1 & 2 AS REQUIRED)		
3	SHORT	.2V DC	–IBIAS
	(DISCONNECT METER USE DISPLAY)		
4.	SHORT	2V DC	POL (±)
5.	+100 μV	2V DC	+ FEED FWD (+10 DIGITS)
6.	–100 μV	2V DC	– FEED FWD (–10 DIGITS)
7.	+1V	2V DC	+2V
8.	+1.9V	2V DC	LIN
	(REPEAT 7 & 8 AS REQUIRED)		
9.	–1.9V	2V DC	–2V
10.	SHORT	.2V DC	FRONT PANEL OFFSET ZERO
11.	+.19	.2V DC	.2V
12.	SHORT	20V DC	HV OFFSET
13.	+1000V	1 KV DC	1 KV
14.	+190V	200V DC	200V
15.	+19V	20V DC	20V
16.	+1000V	1 KV DC	1 KV

(NOTE: IF READJUSTED, REPEAT 14 & 15)

4-WIRE OHMS ADJUSTMENT ⚠

	INPUT	MODE	ADJUST
1.	10 KΩ	20 KΩ	20 KΩ
2.	1 KΩ	2 KΩ	2 KΩ
3.	10 MΩ	20 MΩ	20 MΩ

MODEL 5100 DMM

⚠ REFER TO MANUAL FOR DETAILS

WARNING: GUARD VOLTAGE PRESENT ON COVER

Figure 5.4 - Calibration Points

5.3.9 Calibration Procedure.

5.3.9.1 This procedure is designed to produce the highest accuracy in the least number of steps, while minimizing interaction between adjustments. To insure optimum accuracy, no deviation from the order of adjustments in this procedure can be made.

5.3.9.2 ISOLATOR ZERO.

a. Connect a jumper to J101 (Hi) and J102 (Lo) input terminals. J105 (GUARD) is to be connected to J102 (Lo).

b. Set the DMM to the DCV function and .1 range (manual).

c. Connect a microvoltmeter "Hi" input lead to TP1, isolator output on the reference isolator PCB. A hole in the top cover, labeled "ISO OUT," provides access to the TP1 pin using an insulated minigator or capture type test clip. The microvoltmeter "Lo" input lead is connected to the J102/J105 input terminal (analog common).

d. Adjust the FRONT PANEL ZERO, R32, for zero ± 5 μV.

e. Replace the jumper with a 1 MΩ, 5%, 1/4W resistor.

f. Adjust R8, +I (current) Bias, on the Reference Isolator PCB for zero ± 5 μV.

g. Replace the 1 MΩ resistor with a jumper and repeat steps d, e, and f.

h. Remove the microvoltmeter test leads.

5.3.9.3 POLARITY ADJUSTMENT.

a. With the DMM in the DCV function and the input shorted, select the 1 volt range (manual).

b. Visually monitor the DMM polarity LED, and adjust R33, labeled "POL," on the Digitizer PCB for the center of polarity.

NOTE

The center of polarity is the mid-point of the hysteresis when the polarity indicator "bounces" plus and minus approximately 50% of the readings.

5.3.9.4 FEED FORWARD ADJUSTMENT.

a. With the DMM in the DCV function and 1 volt range (manual). Remove the jumper at the input and connect a DC voltage source set to +100 μV.

b. Adjust R24, labeled + FEED FWD, on the Digitizer PCB for a readout of +0.00010 on the display.

c. Reverse the polarity of the input signal (−100 μV). Adjust R23, labeled − FEED FWD, for a readout of −0.00010 on the display. Recheck the Feed Forward adjustments.

d. Apply a +1.00000 volt to the input terminals and adjust R32, labeled +2V, on the Reference Isolator PCB for a readout of +1.00000 on the display.

e. Increase the input voltage to +1.90000. Adjust R42, labeled LIN, on the Digitizer PCB for a readout of +1.90000 on the display.

f. Repeat steps d and e until each step is within ±1 digit of the required reading on the display.

g. Apply a −1.90000 volts to the input terminals and adjust R1, labeled −2V, on the Digitizer PCB for a readout of −1.90000 on the display.

h. Decrease the input voltage to −1.00000 and verify the readout on the display is −1.00000 ± 5 digits.

i. Check steps a through g and adjust, if necessary.

5.3.9.5 RATIO X10.

a. Set the DMM to DCV and Ratio functions and the 1 volt range (manual). Connect the DMM as shown in the figure 5.5 test setup. Set the divider to .1900000 and adjust the DC voltage standard to +2.000000 volts for the input to the divider and to J103 (EXT REF HI) and J104 (EXT REF LO). Connect the output of the divider to J103 (Hi) and J102/J105 (Lo).

NOTE

Shorting links on the input terminals from J101 to J103 and J102 to J104 must be disconnected before ratio measurements are attempted.

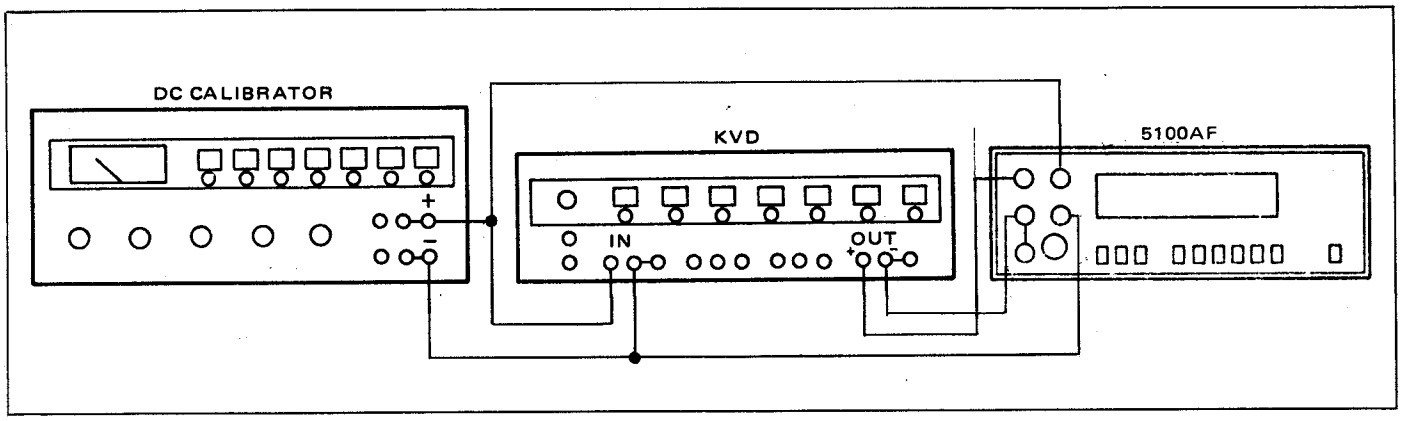


Figure 5.5 - Ratio Test Hookup

b. Adjust R53, Ref OP AMP voltage zero, for a +1.90000 readout on the display. It may be necessary to use the measurement 3-pole active filter (S6) to optimize the adjustment of R53. Take the DMM out of the Ratio function by disabling the Ratio switch (S5).

c. Set the DC voltage standard to +10 volts. The DMM is now in DCV and the 1 range with a +1.90000 volts applied to the input. Adjust R32, labeled +2V, on the Reference Isolator PCB for a readout of +1.90000 on the display.

d. Repeat steps a through c and readjust as necessary.

e. Enable the Ratio switch to place the DMM in Ratio X10, 1 volt range, and adjust R33, ratio linearity adjust, on the Reference Isolator PCB for a readout of +1.90000 on the display.

f. Recheck steps b, c, d, and e and readjust as necessary. Take the DMM out of Ratio by disabling the Ratio Switch (S5), returning the DMM to DCV function, 1 range.

g. Remove the External Reference input cabling.

5.3.9.6 DCV RANGE ADJUSTMENTS.

a. Select the .1 range (manual). Remove the signal input cable, replace with a jumper at J101 and J102/J105, and adjust R32, FRONT PANEL ZERO, for a readout of .000000 ± 1 digit on the display, if necessary.

b. Remove the jumper, apply a +.190000 volt input, and adjust R48, labeled .2V, on the Reference Isolator PCB for a readout of +.190000 on the display.

c. Reverse the polarity input (−.190000 volts) and verify a readout of −.190000 ± 2 digits on the display.

d. Select the 1 volt range, replace the signal input with a jumper, and verify a readout of (±) 0.00000 on the display. Repeat steps a, b, and c, if the readout is not zeroes.

e. Select the 10 volt range, replace the signal input with a jumper and adjust R16, labeled HV OFFSET, on the Digitizer PCB for a readout of (±) 00.0000 on the display. Remove the input jumper.

f. Select the 1000 range, apply a +1000.00 volts to the input terminals (J101 and J102/J105). Adjust R57, labeled 1 KV, on the Digitizer PCB for a readout of +1000.00 on the display.

g. Reduce the DC voltage standard to +190.000 volts at the input terminals and select the 100 volt range (manual). Adjust R50, labeled 200V, on the Digitizer PCB for a readout of +190.000 on the display.

h. Reduce the DC voltage standard to +19.0000 volts at the input terminals and select the 10 volt range (manual). Adjust R55, labeled 20V, on the Digitizer PCB for a readout of +19.0000 on the display.

i. Repeat steps f, g, and h and readjust, if necessary.

j. Reduce the voltage standard outputs and remove input cables.

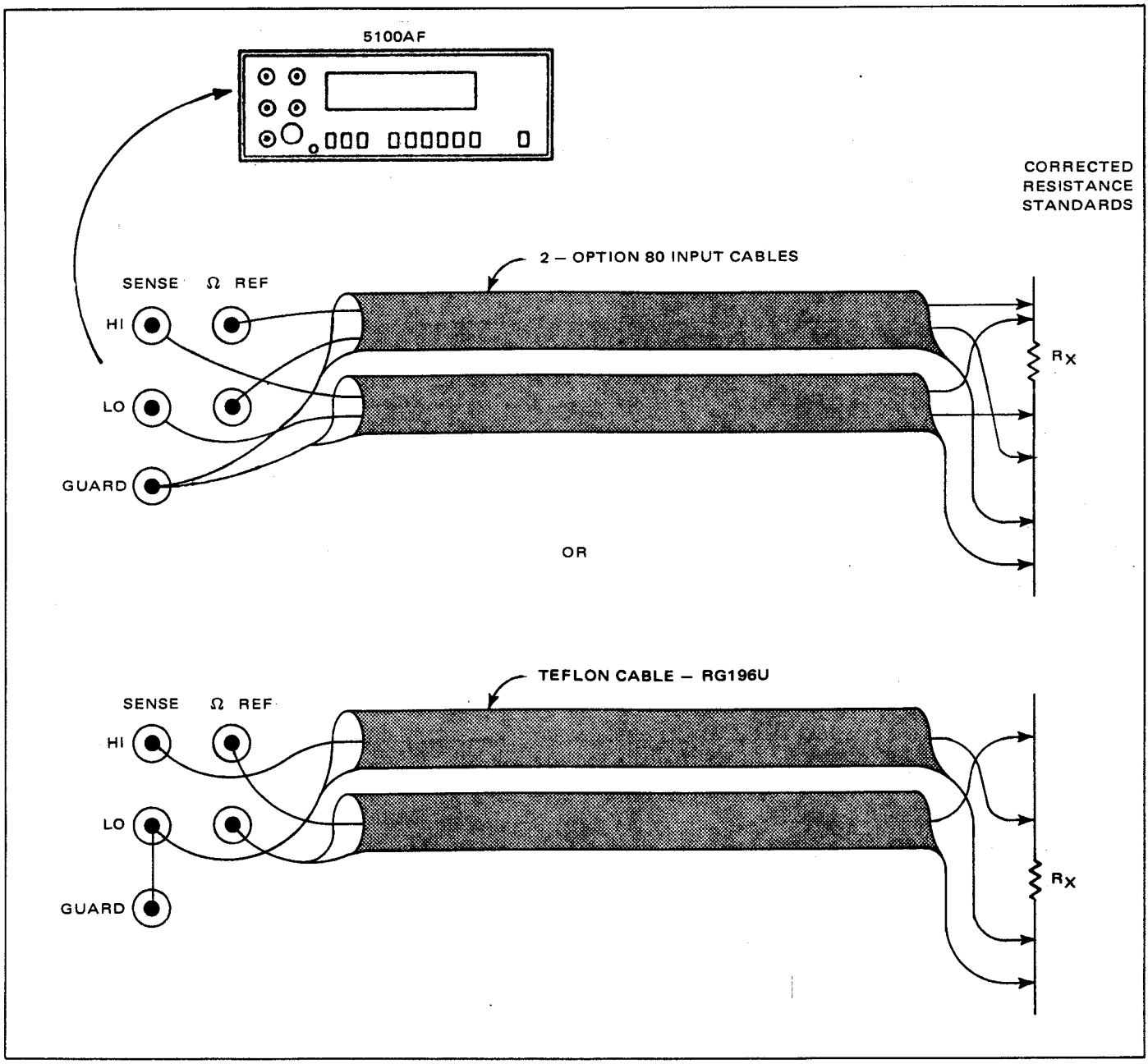


Figure 5.6 - Ohms Measurement Connection

5.3.9.7 4-WIRE KOHMS ADJUSTMENTS.

NOTE

Low sense line must be less than 1 ohm.

a. With the DMM in the DCV function, select the .1 volt range. Connect a jumper to the input terminals and adjust R32, FRONT PANEL ZERO, for a readout of (±) .000000 on the display, if necessary.

b. Connect the DMM as shown in the figure 5.5 test setup.

c. Select the Kohms function and the 10 Kohm range. Connect the DMM to a 10 Kohm resistance standard using a 4-wire, low leakage cable as shown in figure 5.6.

d. Adjust R31, labeled 20 KΩ, on the Reference Isolator for a readout equal to the resistance standard value.

e. Connect the DMM to a 1 Kohm resistance standard, select the 1 Kohm range, and adjust R56, labeled 2 KΩ, on the digitizer PCB for a readout equal to the resistance standard value.

f. Connect the DMM to a 100 ohm resistance standard, select the .1 Kohm range, and verify that the readout is equal to the value of the resistance standard, ± 32 digits.

g. Set the DMM to the 100 Kohm range, connect the DMM input to a 100 Kohm resistance standard, and verify that the readout is equal to the value of the resistance standard, ± 32 digits.

h. Set the DMM to the 1000 Kohm (1 MΩ) range, connect the DMM input to a 1 Mohm resistance standard, and verify that the readout is equal to the value of the resistance standard, ± 32 digits.

i. Set the DMM to the 10,000 Kohm (10 MΩ) range, connect the DMM input to a 10 Mohm resistance standard, select the measurement 3-pole filter, and adjust R39, labeled 20 MΩ, on the digitizer PCB for a readout of 10.0000 on the display.

j. Remove the input cables from the DMM and resistance standard and disable the measurement filter.

5.3.9.8 AC CONVERTER (Averaging).

a. Select the ACV function and the 1000 range. Connect the AC voltage standard source set to 1000V AC @ 1 kHz to the input terminals, J101 (Hi) and J102/J105 (Lo). Adjust R10, labeled 1 KV LF, on the AC converter for a readout of 1000.00 on the display.

b. Increase the frequency of the AC voltage standard to 20 kHz and adjust C2, labeled 1 KV HF, on the AC converter for a readout of 1000.00 on the display.

c. Reduce the output of the AC voltage standard to 1V AC @ 1 kHz, select the 1 volt range, and adjust R19, labeled 2V LF, on the AC converter for a readout of 1.00000 on the display.

d. Increase the frequency of the AC voltage standard to 20 kHz and adjust C5, labeled 2V HF, on the AC converter for a readout of 1.00000 on the display.

e. Select the 10 volt range, increase the output of the AC voltage standard to 10.0000 volts @ 1 kHz, and adjust R21, labeled 20V LF, on the AC converter for a readout of 10.0000 on the display.

f. Increase the frequency of the AC voltage standard to 20 kHz and adjust C7, labeled 20V HF, on the AC converter for a readout of 10.0000 on the display.

g. Select the 100 volt range, increase the output of the AC voltage standard to 100.000 volts @ 1 kHz and adjust R23, labeled 200V LF, on the AC converter for a readout of 100.000 on the display.

h. Increase the frequency of the AC voltage standard to 20 kHz and adjust C9, labeled 200V HF, on the AC converter for a readout of 100.000 on the display.

5.4 TROUBLESHOOTING PERFORMANCE TESTS.

5.4.1 This section contains Unit and Subassembly performance tests. The unit performance tests are designed to isolate a malfunction to a replaceable module or printed circuit board. In some cases where the printed circuit board is large and complex, the unit test is designed to isolate the malfunction to a functional area of the board.

The unit performance tests are organized by instrument function such as AC volts, DC volts or Kohms. A "singlethread" diagram is provided for each of the unit performance tests. These diagrams show the primary signal path through the instrument for the individual function of the instrument.

5.4.2 The subassembly performance tests are designed to isolate a malfunction to a component or small group of components on a printed circuit board.

These tests are organized by subassembly such as the display PCB or the AC converter board.

5.4.3 Both the unit and subassembly performance tests present test setup instructions, step by step instructions for monitoring the circuit under test and performance standards in the form of voltage levels or oscilloscope waveforms. In addition the tests are fully illustrated by either the "singlethread" diagrams or schematics which illustrate the test point location within the circuit under test. For ease in locating the physical test point within the instrument, pictorial drawings are provided on pages facing the schematic.

5.4.4 Test points called out in the performance tests may be actual physical test points provided as convenience test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares or diamonds. These "flags" also appear on the corresponding schematic and on the pictorial drawing in the Drawing section of this manual.

5.4.5 Note that the test points are numbered sequentially so as to start at the input of a circuit and progress to the output. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to square black test point flags 1 appearing on the assembly drawing and schematics in the Drawing Section (6). These black square test point flags indicate voltage measurement points. Similarly the alphabetic test points refer to black diamond shaped flags A appearing on the assembly drawings and schematics. The Alphabetic diamond flags indicate oscilloscope test points.

5.4.6 To perform subassembly performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors and capacitors in and around the area of malfunction.

5.4.7 Unit Performance Tests.

5.4.8 Tables 5.6 through 5.9 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements. Troubleshooting, unlike calibration, may be done with any equipment that is accurate to 5%.

5.4.9 The performance tests presented in this section are:

DC Volts Unit Performance Test	Table 5.6
DC 3-Wire Ratio (X10) Unit Performance Test	Table 5.7
AC Volts (Averaging) Unit Performance Test	Table 5.8
Kohms Unit Performance Test	Table 5.9

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

Table 5.6 - DCV Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .1 (manual) Input Terminals: J10 (Hi) and J102 (Lo) connected to a DC voltage standard set to ±0.10000V					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Use of DC active filter, S6, optional. NOTE: Guard (J105) to be strapped to Sig Lo (J102).
	DC Voltage Input	S1-B-2	1		±0.100000V DC ± Tol.
	Isolator Input	E26	2		±0.100000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		±1.00000V DC ± Tol.
Range: 1 (manual) Set DC voltage standard to ±1.00000V	DC Voltage Input	S1-B-2	1		±1.00000V DC ± Tol.
	Isolator Input	E26	2		±1.0000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		±1.00000V DC ± Tol.
Range: 10 (manual) Set DC voltage standard to ±10.0000V	DC Voltage and HV Buffer Input	S2-B-2	4		±10.0000V DC ± Tol.
	Attenuator Input	S2-A-2	5		±10.0000V DC ± Tol.
	Attenuator and Isolator Input	E26	2		±1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		±1.00000V DC ± Tol.
Range: 100 (manual) Set DC voltage standard to ±100.000V	DC Voltage and HV Buffer Input	S2-B-2	4		±100.000V DC ± Tol.
	Attenuator Input	S2-A-2	5		±100.000V DC ± Tol.

Table 5.6 - DCV Unit Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Attenuator Output and Isolator Output	E26	2		±1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		±1.00000V DC ± Tol.
Range: 1000 (manual) Set DC voltage standard to ±1000.00V	DC Voltage Input and 9 MΩ Divider Resistor	S3-B-2	6		±1000.00V DC ± Tol.
	Attenuator Input	S2-A-2	5		±100.000V DC ± Tol.
	Attenuator Output and Isolator Input	E26	2		±1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		±1.00000V DC ± Tol.
Reduce DC voltage standard to 0V					

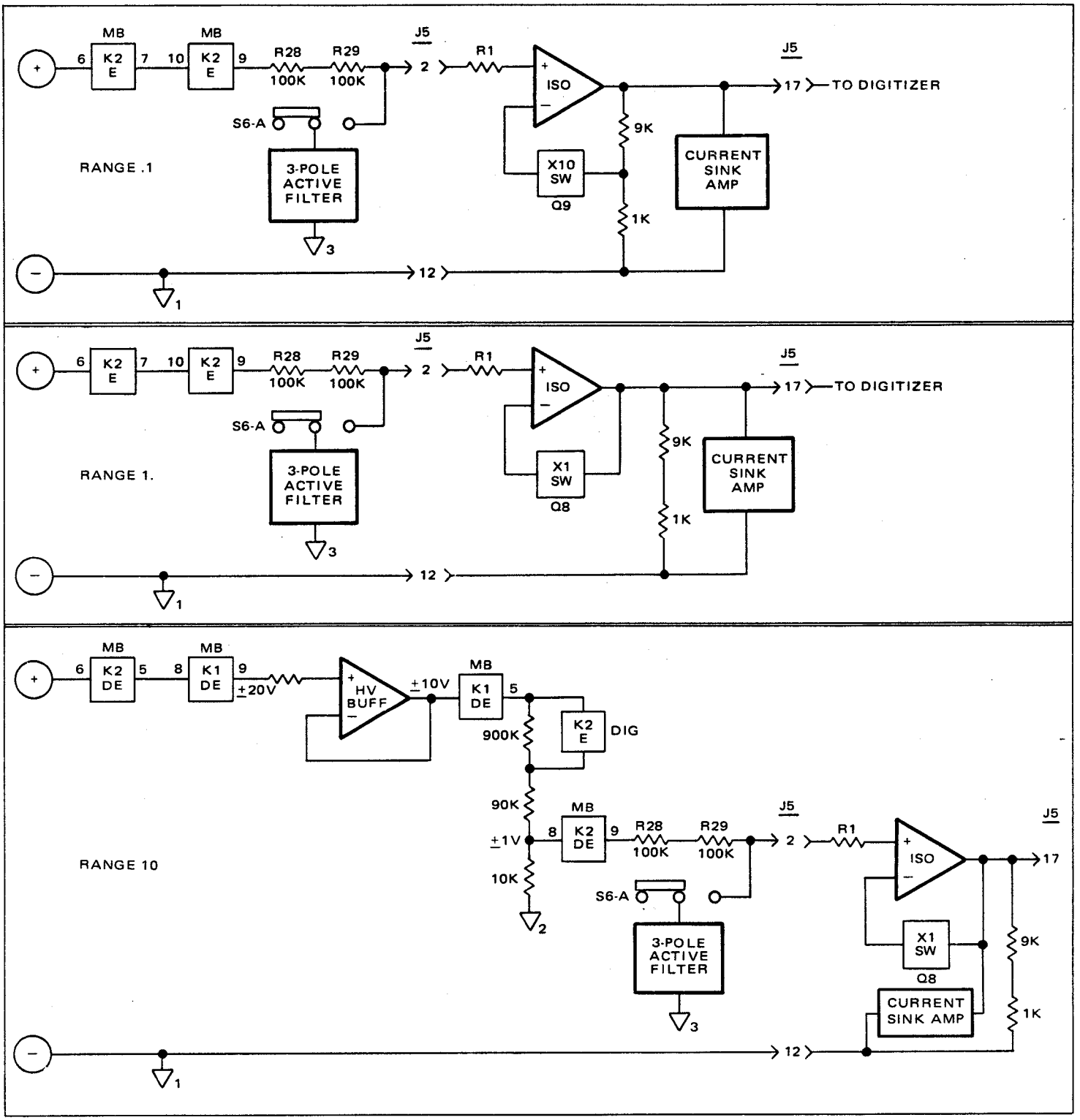


Figure 5.7 - DCV Simplified Schematic; .1, 1., 10 Volt Ranges

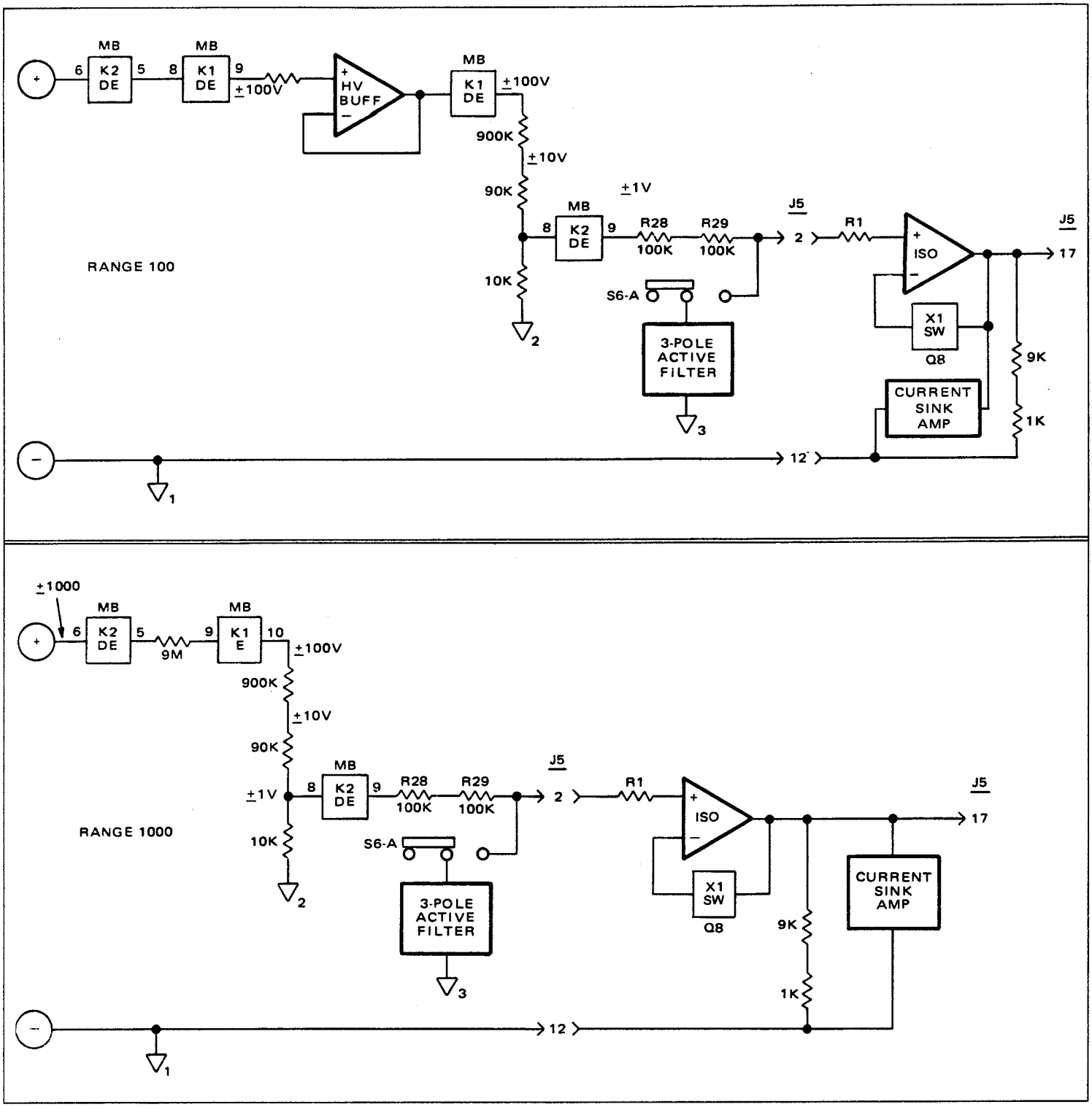
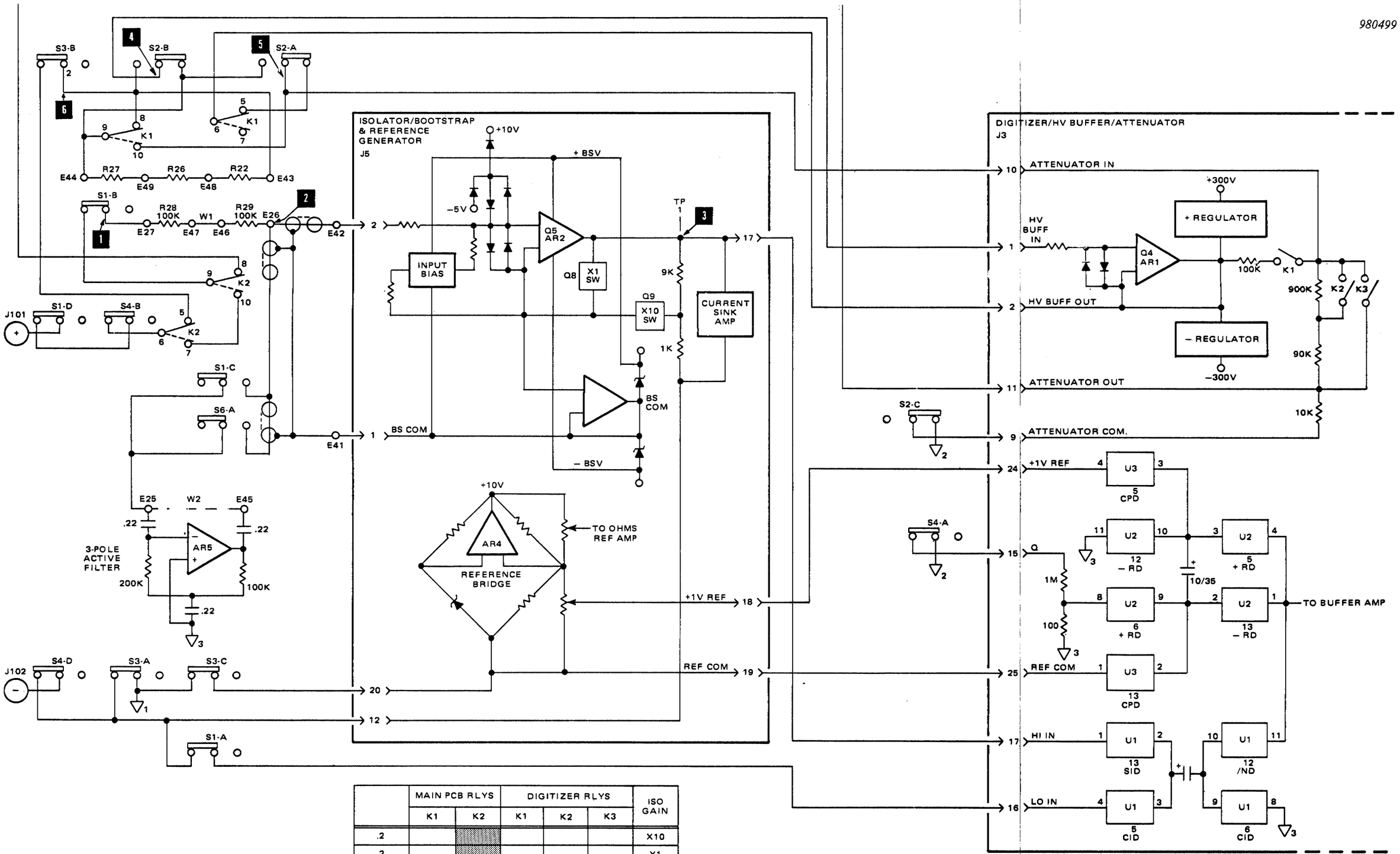


Figure 5.8 - DCV Simplified Schematic; 100 and 1000 Volt Ranges



	MAIN PCB RLYS		DIGITIZER RLYS			ISO GAIN
	K1	K2	K1	K2	K3	
.2		■				X10
2		■				X1
20				■		X1
200						X1
1000	■					X1

■ ENERGIZED

Figure 5.9 - DCV Single Thread Diagram

Table 5.7 - 3-Wire Ratio (X10) Unit Performance Test

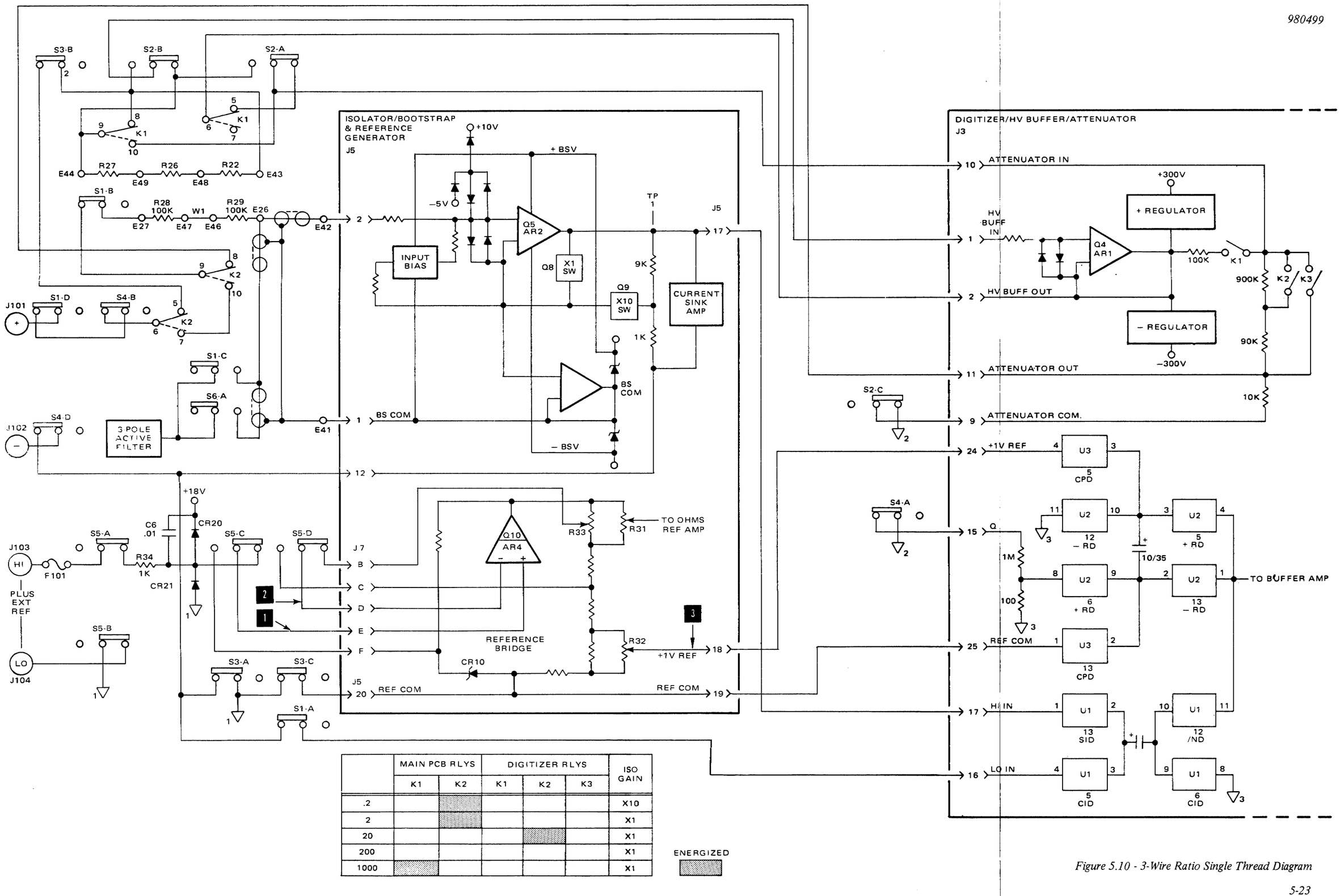
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV (S2) & RATIO (S5) Range: .1 (manual) Input Terminals: Signal Input, J101 (Hi) and J102 (Lo) connected to a DC voltage standard set to ±.1 volts. Reference input, J103 (Hi) and J104 (Lo) connected to a DC voltage standard set to +10 volts.					NOTE: The ratio technique used is 3-wire. When using a negative input signal, be careful to avoid ground loops and unreferenced power levels to prevent shock hazards to the operator and possible damage to associated test equipment.
					NOTE: Shorting links between J101 & J103, J102 & J104 must be disconnected before a ratio measurement can be made
					NOTE: See DCV unit performance test (Table 5.6)
					NOTE: All measurements are referenced to TP4 (MECCA)
					NOTE: Guard (J105) to be connected to Sig Lo (J102)
					NOTE: Use of the DC active measurement filter (S6) optional
Display: ±.100000	Ref Op Amp + In	J7-E	1		+10.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+10.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+1.0000V DC ± Tol
Reference Input set to +9 volts. Display: ±.111111	Ref Op Amp + In	J7-E	1		+9.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+9.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.9000V DC ± Tol
Reference Input set to +8 volts. Display: ±.125000	Ref Op Amp + In	J7-E	1		+8.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+8.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.8000V DC ± Tol

Table 5.7 - 3-Wire Ratio (X10) Unit Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Reference Input set to +7 volts. Display: ±.142857	Ref Op Amp + In	J7-E	1		+7.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+7.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.7000V DC ± Tol
Reference Input set to +6 volts. Display: ±.133333	Ref Op Amp + In	J7-E	1		+6.000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+6.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.6000V DC ± Tol
Reference Input set to +5 volts. Display: ±.199999 or ±0.20000	Ref Op Amp + In	J7-E	1		+5.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+5.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.5000V DC ± Tol
Reference Input set to +4 volts. Display: ±0.25000	Ref Op Amp + In	J7-E	1		+4.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+4.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.4000V DC ± Tol
Reference Input set to +3 volts. Display: ±0.33333	Ref Op Amp + In	J7-E	1		+3.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+3.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.3000V DC ± Tol
Reference Input set to +2 volts. Display: ±0.50000	Ref Op Amp + In	J7-E	1		+2.0000V DC ± Tol
	Ref Op Amp – In	J7-D	2		+2.0000V DC ± Tol
	+1V Ref Out	J5-18	3		+0.2000V DC ± Tol
Disable Ratio sw (S5) to DCV Function, reduce input voltages and remove cables.					

Signal Range	Ratio X10	Ext Ref Voltage DC
±.1	.01:1	+2V to +10V
±1	.1:1	+2V to +10V
±10	1:1	+2V to +10V
±100	10:1	+2V to +10V
±1000 (±1100V max)	100:1*	+5V to +10V

*100:1 ratio X10, using a ±1000V DC signal, must use an external reference voltage of +5 volts or greater to obtain a valid display. Voltages less than +5 volts will cause overrange, "200000" flashing at read rate.



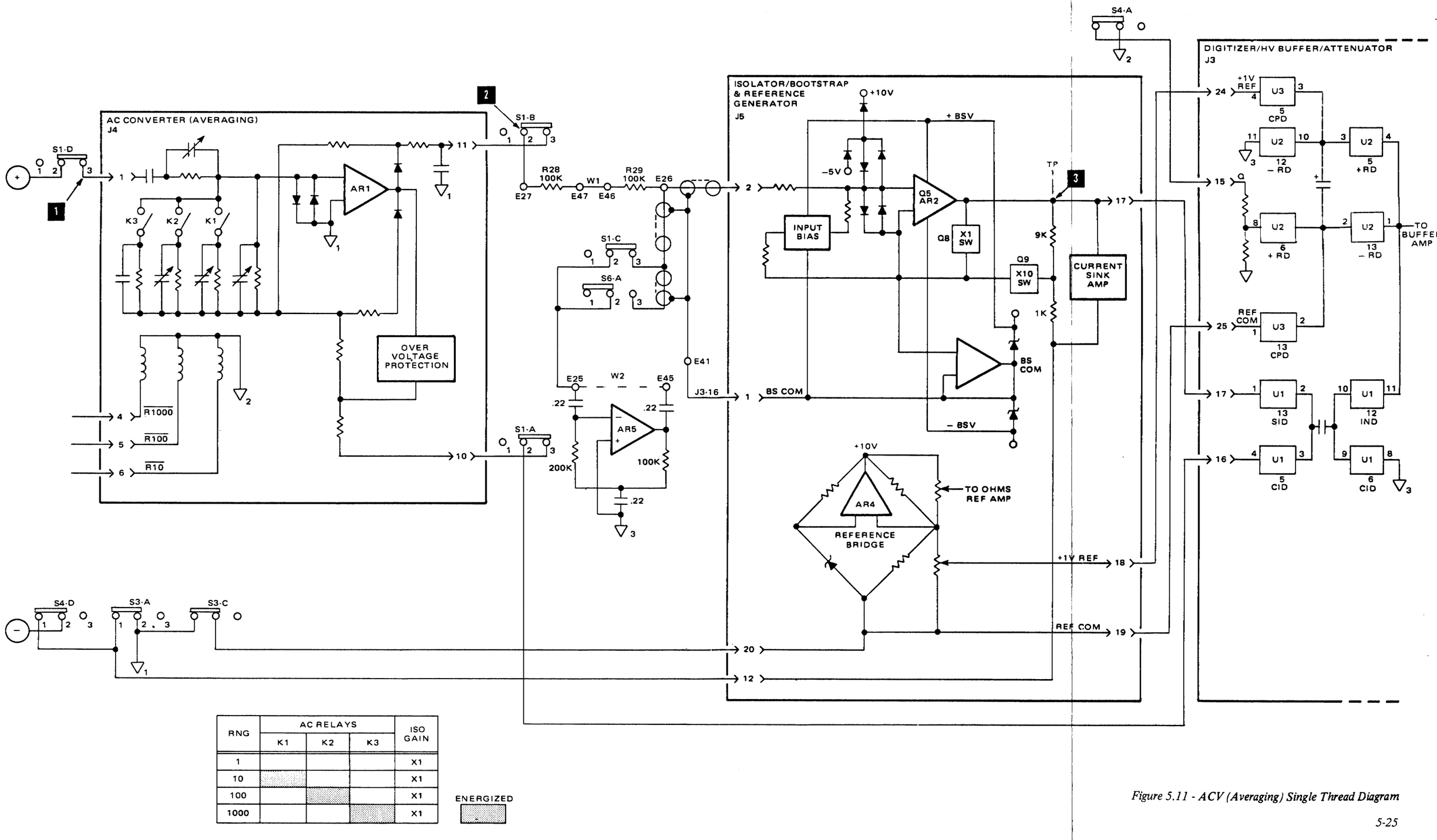
	MAIN PCB RLYS		DIGITIZER RLYS			ISO GAIN
	K1	K2	K1	K2	K3	
.2		■				X10
2		■				X1
20				■		X1
200						X1
1000	■					X1

■ ENERGIZED

Figure 5.10 - 3-Wire Ratio Single Thread Diagram

Table 5.8 - ACV (Averaging) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV **Range:** 1 (manual) **Input Terminals: J101 (Hi) and J102 (Lo) connected to an AC voltage standard set to** 1.00000V @ 10 kHz					NOTE: All measurements are referenced to TP4 (MECCA)
					NOTE: Frequency of input signal optional
					NOTE: Guard (J105) to be strapped to Sig Lo (J102)
	AC Signal Input	S1-D-3	1		1.0000V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 10 (manual) Set AC voltage standard to 10.0000V @ 10 kHz	AC Signal Input	S1-D-3	1		10.0000V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 100 (manual) Set AC voltage standard to 100.000V @ 10 kHz	AC Signal Input	S1-D-3	1		100.000V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 1000 (manual) Set AC voltage standard to 1000V @ 10 kHz	AC Signal Input	S1-D-3	1		1000.00V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Reduce AC voltage standard to 0V					



RNG	AC RELAYS			ISO GAIN
	K1	K2	K3	
1				X1
10				X1
100				X1
1000				X1

ENERGIZED

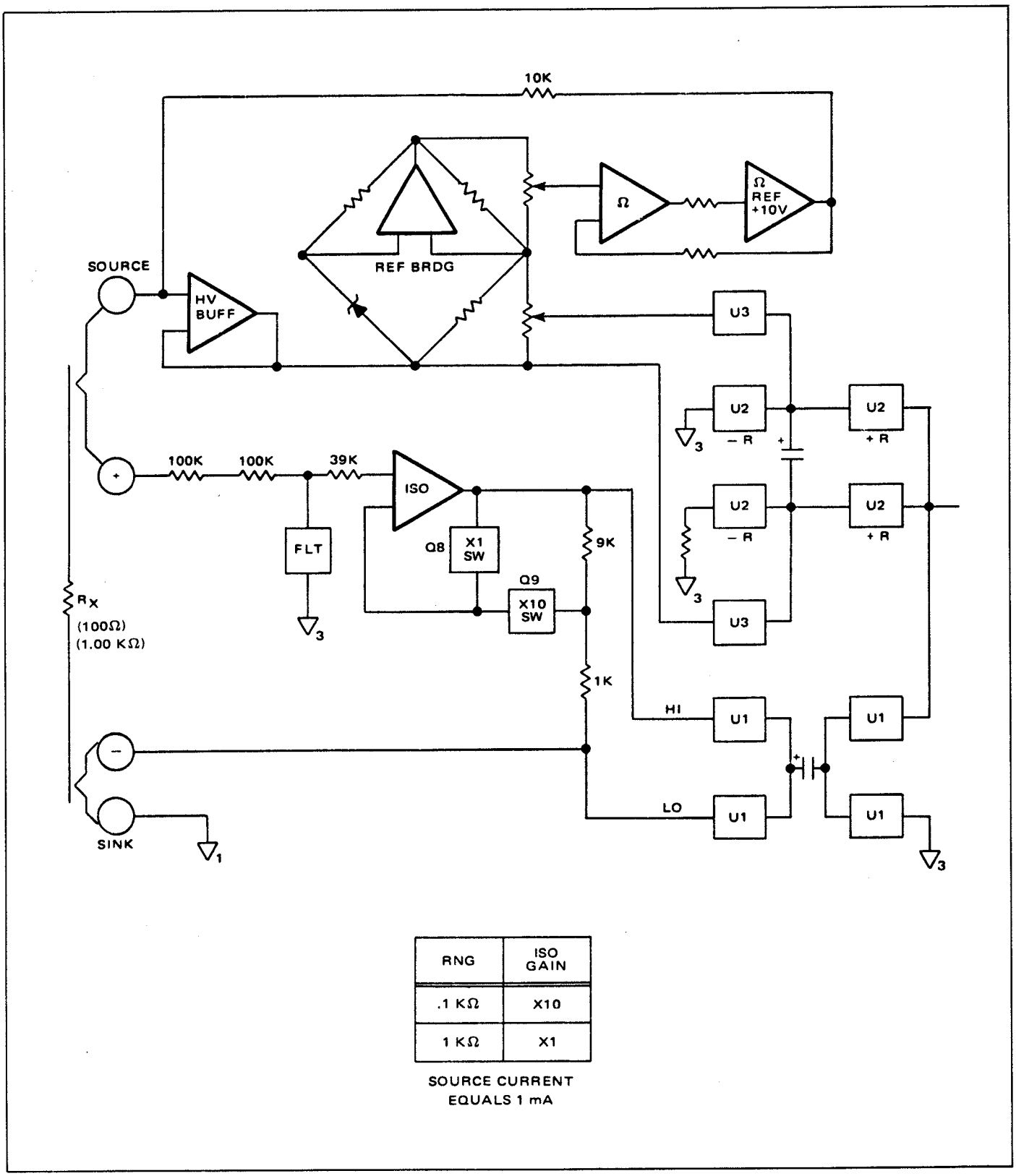
Figure 5.11 - ACV (Averaging) Single Thread Diagram

Table 5.9 - Kohms Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: KΩ **Range:** .1 (manual) **Input Terminals: J101 (Hi)/J103 (Ω Source) and J102 (Lo)/J104 (Ω -Sink) connected to a resistance standard set to** 100.00Ω					NOTE: All measurements are referenced to TP4 (MECCA)
					NOTE: Guard (J105) to be strapped to Sig Lo (J102)
					NOTE: Use of the DC active filter, S6, is optional
	KΩ Reference Voltage	S2-C-1	1		+10.1000V DC ± Tol.
	Isolator Input	S1-B-2	2		+0.10000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 1 (manual) **Set resistance standard to** 1.00 KΩ	KΩ Reference Voltage	S2-C-1	1		+11.000V DC ± Tol.
	Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 10 (manual) **Set resistance standard to** 10.0 KΩ	KΩ Reference Voltage	S2-C-1	1		+11.000V DC ± Tol.
	Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 100 (manual) **Set resistance standard to** 100 KΩ	KΩ Reference Voltage	S2-C-1	1		+11.000V DC ± Tol.
	Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.

Table 5.9 - Kohms Unit Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Range: 1000 (manual) Set resistance standard to 1.00 MΩ	KΩ Reference Voltage	S2-C-1	1		+11.000V DC ± Tol.
	Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.
Range: 10,000 (manual) Set resistance standard to 10.0 MΩ	KΩ Reference Voltage	S2-C-1	1		+11.000V DC ± Tol.
	Isolator Input	S1-B-2	2		+1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3		+1.00000V DC ± Tol.



RNG	ISO GAIN
.1 KΩ	X10
1 KΩ	X1

SOURCE CURRENT EQUALS 1 mA

Figure 5.12 - Kohms Simplified Schematic; .1Kohm and 1 Kohm Ranges

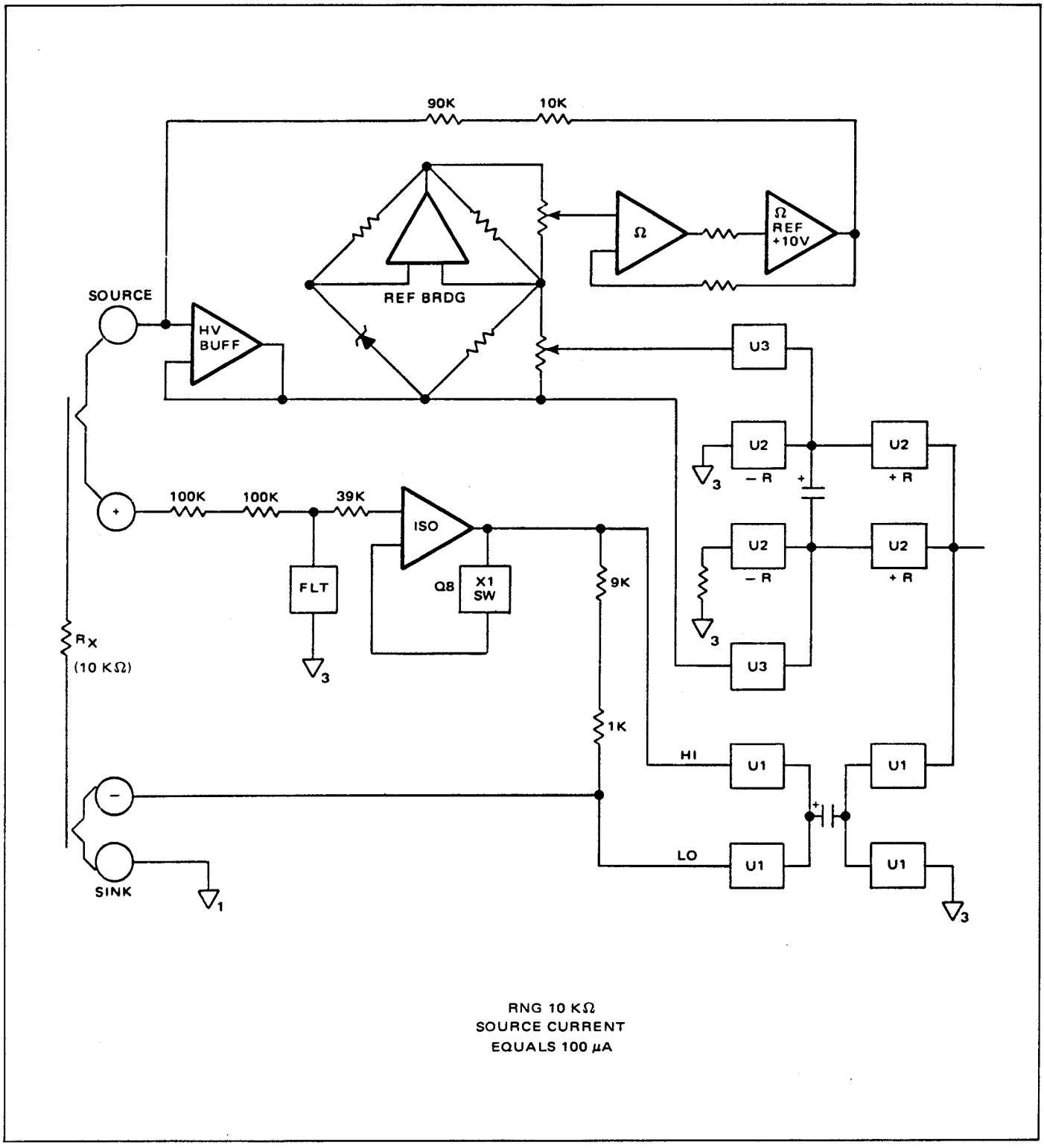


Figure 5.13 - Kohms Simplified Schematic; 10K Ohm Range

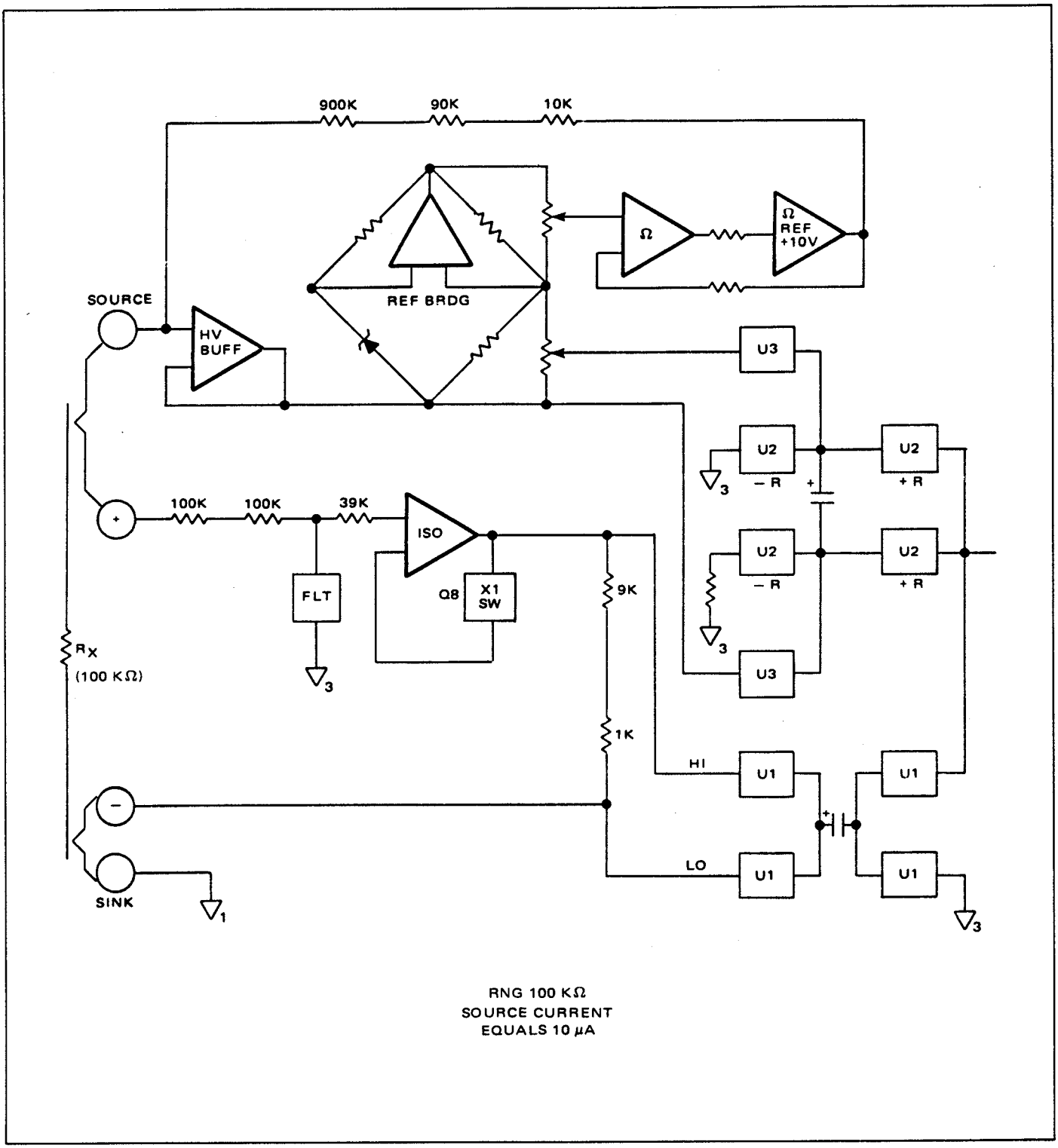


Figure 5.14 - Kohms Simplified Schematic; 100K Ohm Range

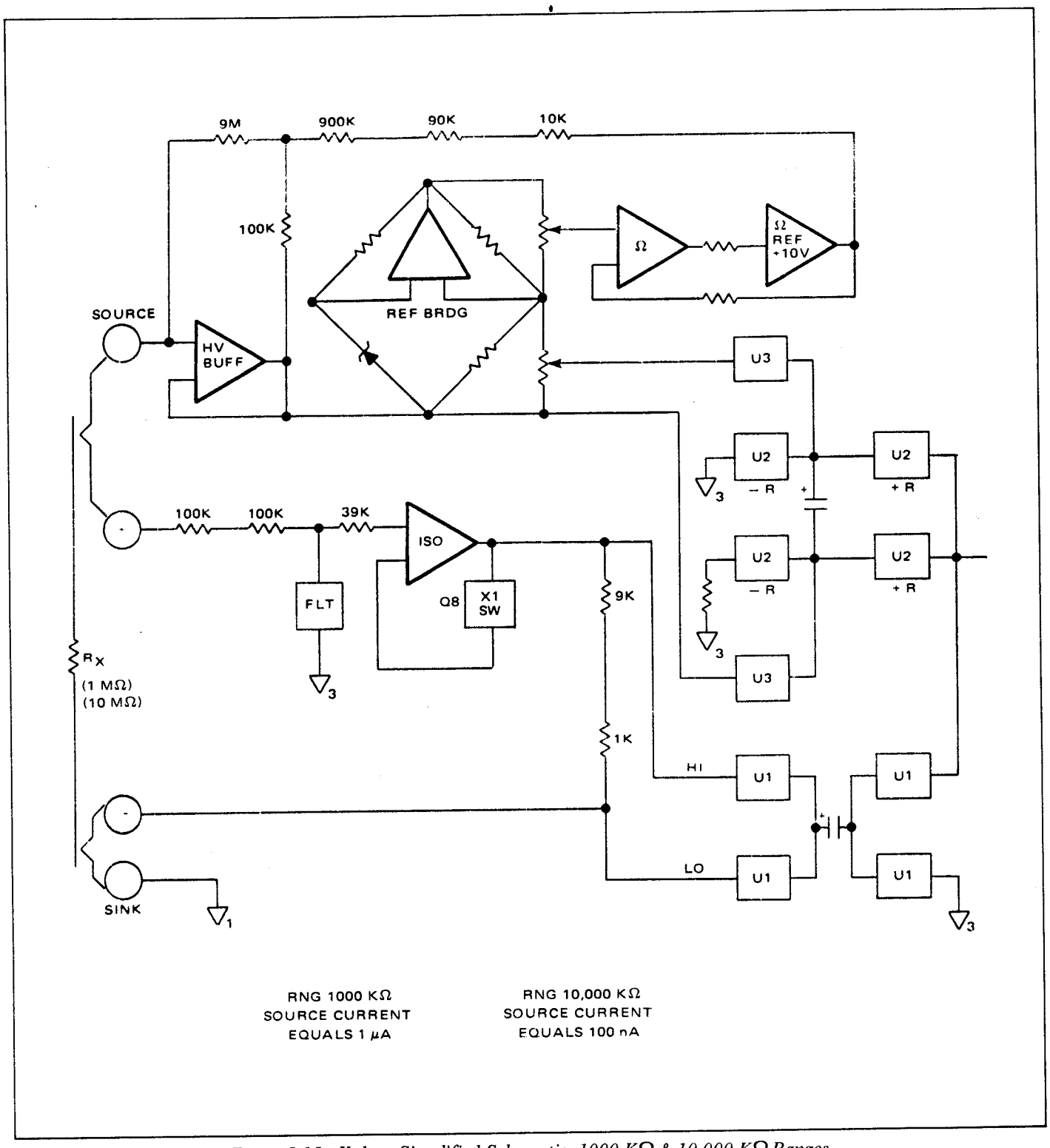
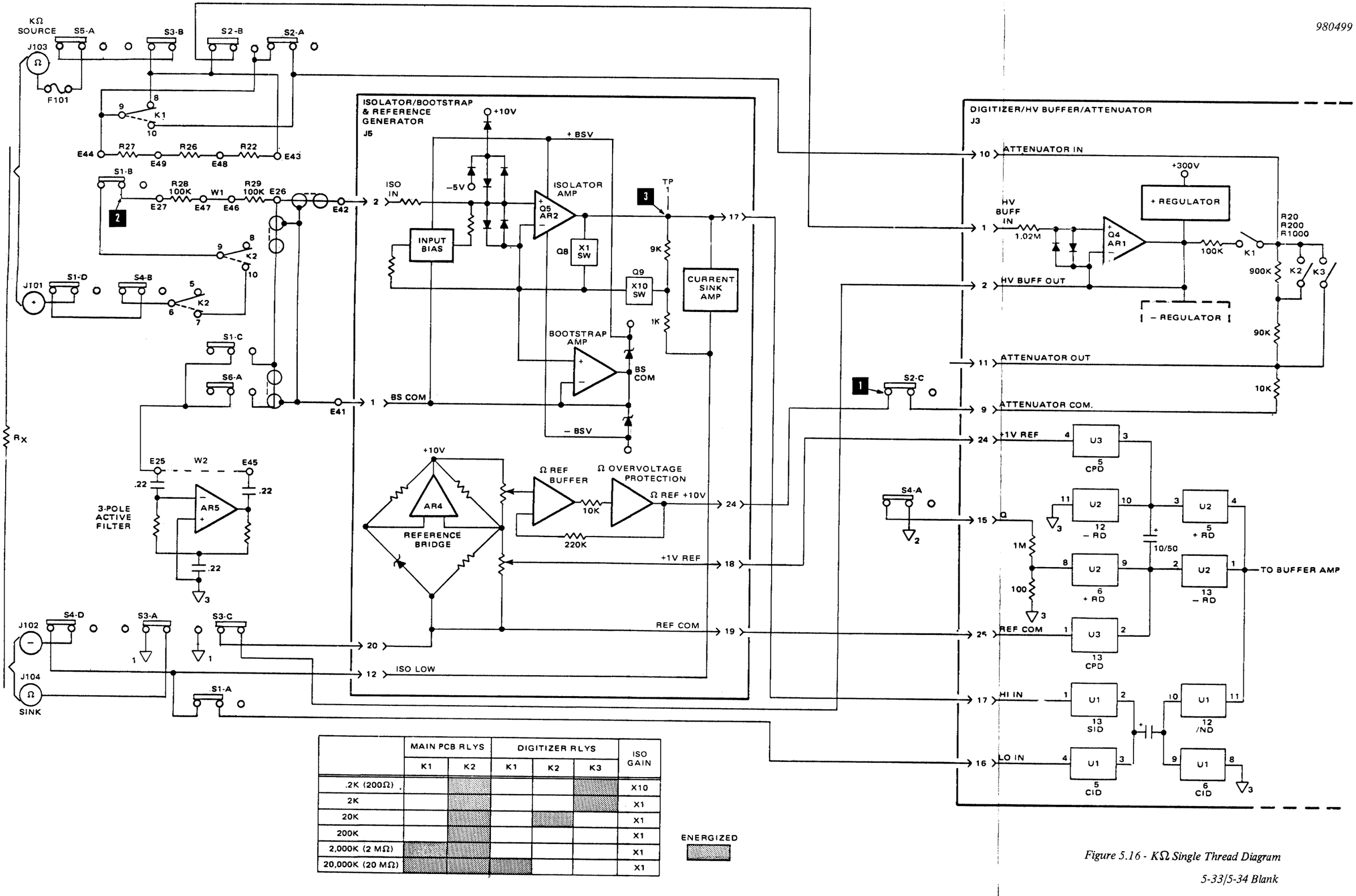


Figure 5.15 - Kohms Simplified Schematic; 1000 KΩ & 10,000 KΩ Ranges



	MAIN PCB RLYS		DIGITIZER RLYS			ISO GAIN
	K1	K2	K1	K2	K3	
.2K (200Ω)		■			■	X10
2K		■			■	X1
20K		■		■		X1
200K		■				X1
2,000K (2 MΩ)	■	■				X1
20,000K (20 MΩ)	■	■	■			X1

■ ENERGIZED

Figure 5.16 - KΩ Single Thread Diagram

5-33/5-34 Blank

5.4.10 Subassembly Performance Tests.

5.4.11 Subassembly performance tests are designed to isolate a malfunction to a small group of components or a single functional group of components. Once the trouble is narrowed down to a small area the technician should resort to conventional troubleshooting techniques such as checking individual components such as resistors, capacitors, semiconductors and applying heat and cold to individual components. Each of the subassembly performance tests is accompanied by performance standards for each step of the test. These performance standards are in the form of static DC voltages or waveform pictures.

In the case of the main printed circuit board, the largest and most complex of the PCBs, several performance tests have been provided. These tests are segregated because the main PCB contains a number of separate functional circuits such as the clock, isolator, range control and null detector. Separate performance tests are provided for each of the remaining smaller boards.

5.4.12 Note that the test points in the performance test tables refer to the performance standard or waveforms in the test and to the test point shown on the assembly drawings and schematic drawings in Section 6 of this manual. The presentation of assembly drawings in the troubleshooting section and again in the drawing section of the manual is redundant but it provides the necessary continuity and makes the technicians troubleshooting job easier.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

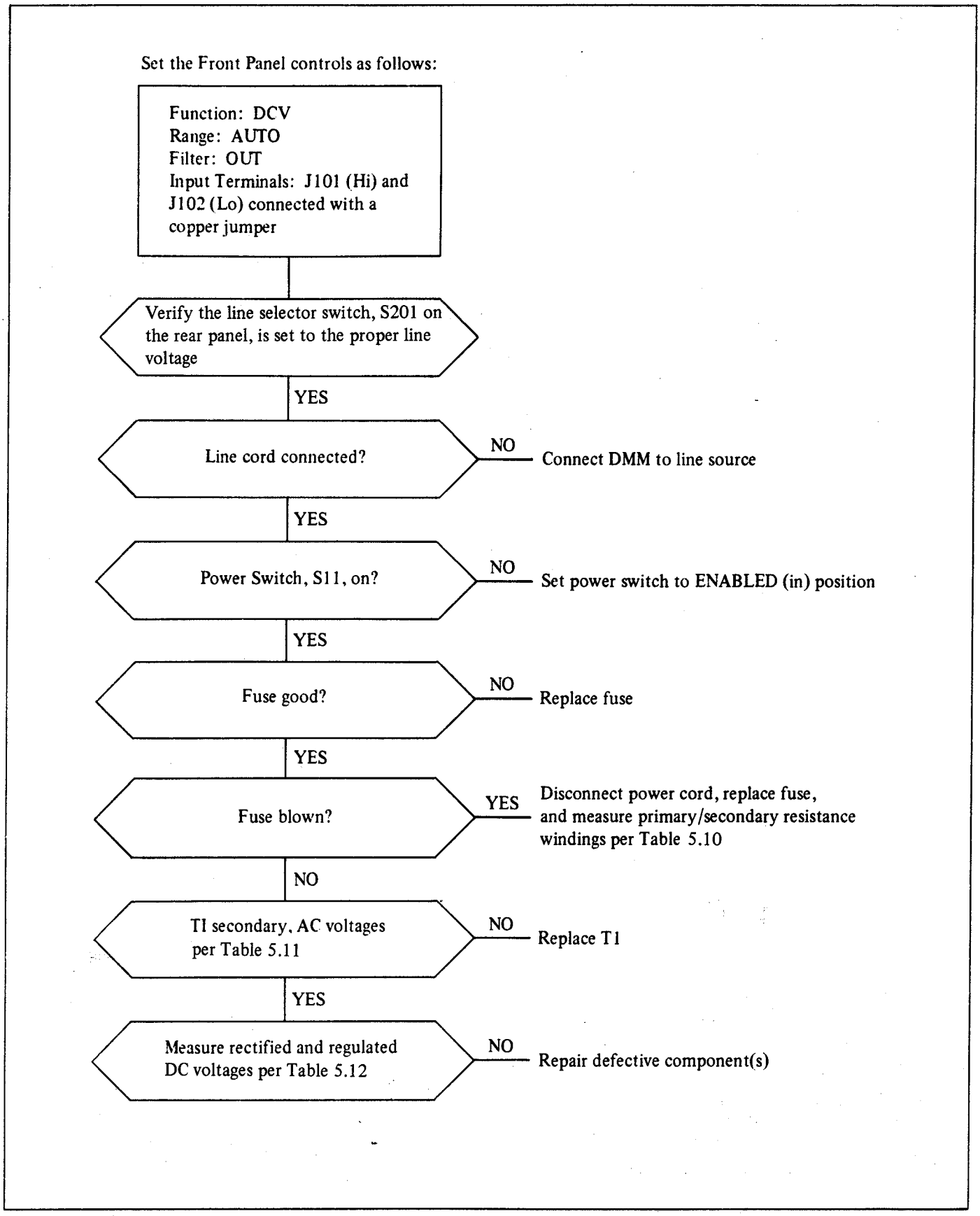


Figure 5.17 - Main PCB, Power Supply Subassembly Performance Test

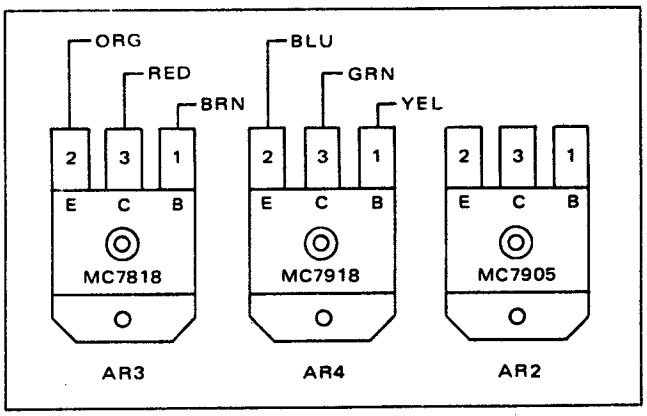


Figure 5.18 - Voltage Regulator Pin Assignments

Table 5.11 - Secondary AC Voltages of T1

From	To	Measurement
T1-6	T1-7	9.5 VAC ± 5%
T1-10	T1-11	205 VAC ± 5%
T1-12	T1-13	7.4 VAC ± 5%
T1-13	T1-14	7.4 VAC ± 5%
T1-12	T1-14	14.75 VAC ± 5%
T1-15	T1-16	37 VAC ± 5%

Table 5.10 - Primary Resistance of T1

J1 Line Select Setting	J201 Line (L) to Neutral (N)
115 VAC	20Ω ± 1Ω
230 VAC	67Ω ± 3Ω

Secondary Resistances of T1		
From	To	Measurement
T1-6	T1-7	2.75Ω ± .5Ω
T1-10	T1-11	495Ω ± 10Ω
T1-12	T1-13	0.65Ω ± 0.15Ω
T1-13	T1-14	0.65Ω ± 0.15Ω
T1-12	T1-14	1.3Ω ± 0.3Ω
T1-15	T1-16	65Ω ± 1Ω

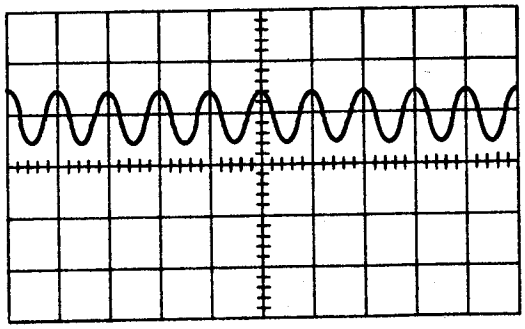
Table 5.12 - DC Voltages Referenced to MECCA (TP4)

Ref Desig	Measurement	P-P Ripple
E34	+255V ± 5V	6V
E35	−255V ± 5V	6V
AR2-3(C)	−7.5V ± 0.3V	700 mV
AR2-2(E)	−5.0V ± 0.25V	15 mV
AR4-3(C)	−22V ± 1V	400 mV
AR4-2(E)	−18V ± 0.5V	10 mV
AR3-1(B)	+22V ± 1V	400 mV
AR3-2(E)	+18V ± 0.5V	10 mV
CR15 (Cathode)	+10V ± 0.5V	5 mV
CR16 (Anode)	−18V ± 1V	20 mV
Q6 (Emitter)	−17V ± 1V	20 mV

Table 5.13 - Main PCB, Oscillator/Clock & MUX Oscillator Subassembly Performance Test

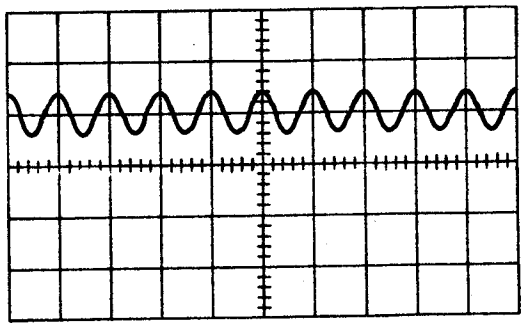
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: AUTO Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP3 (DIG COM).
	Oscillator Output	U1-10/13	A	Figure 5.19	Waveform 1
	Clock Output	U1-2	B	Figure 5.19	Waveform 2
	MUX Osc.	U1-9	C	Figure 5.19	Waveform 3
	MUX Osc.	U1-8/5	D	Figure 5.19	Waveform 4
	MUX Osc.	U1-6/3	E	Figure 5.19	Waveform 5
	MUX Osc. Output	U1-4	F	Figure 5.19	Waveform 6

1 (NO.)
U1-10/13
OSC OUT
2 MHz ± 1%



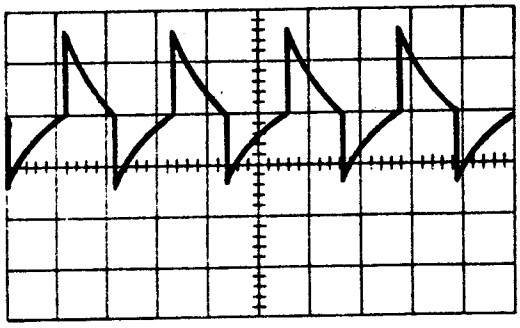
1.0 (V/DIV)
0.5 μS (S/DIV)
REF: DIGITAL COMMON
DC COUPLED

2 (NO.)
U1-2
CLOCK OUT
2 MHz ± 1%



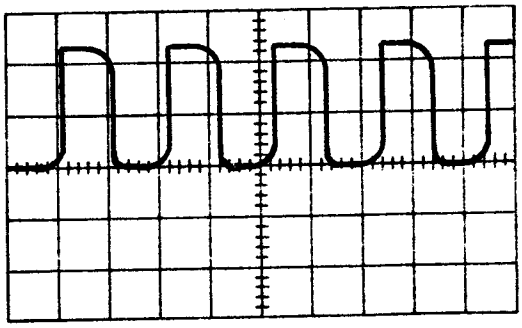
1.0 (V/DIV)
0.5 μS (S/DIV)
REF: DIGITAL COMMON
DC COUPLED

3 (NO.)
U1-9
MUX OSC
500 Hz ± 10%



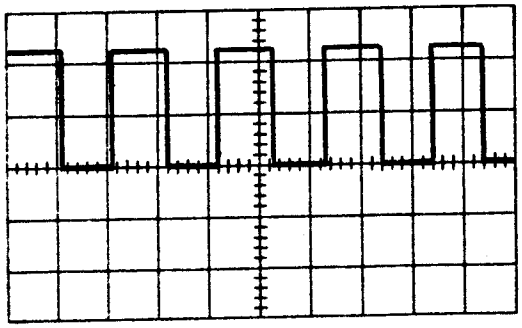
2.0V (V/DIV)
1 mS (S/DIV)
REF: DIGITAL COMMON
DC COUPLED

4 (NO.)
U1-8/5
MUX OSC
500 Hz ± 5%



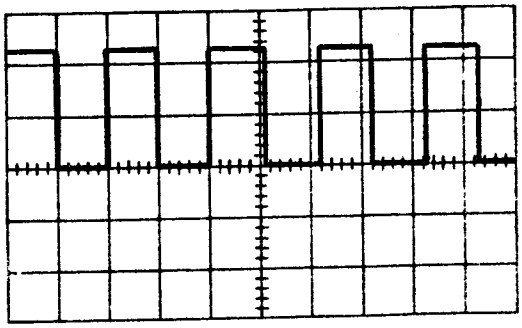
2.0V (V/DIV)
1 mS (S/DIV)
REF: DIGITAL COMMON
DC COUPLED

5 (NO.)
U1-6/3
MUX OSC
500 Hz ± 5%



2.0V (V/DIV)
1 mS (S/DIV)
REF: DIGITAL COMMON
DC COUPLED

6 (NO.)
U1-4
MUX OSC OUT
500 Hz ± 5%



2.0V (V/DIV)
1 mS (S/DIV)
REF; DIGITAL COMMON
DC COUPLED

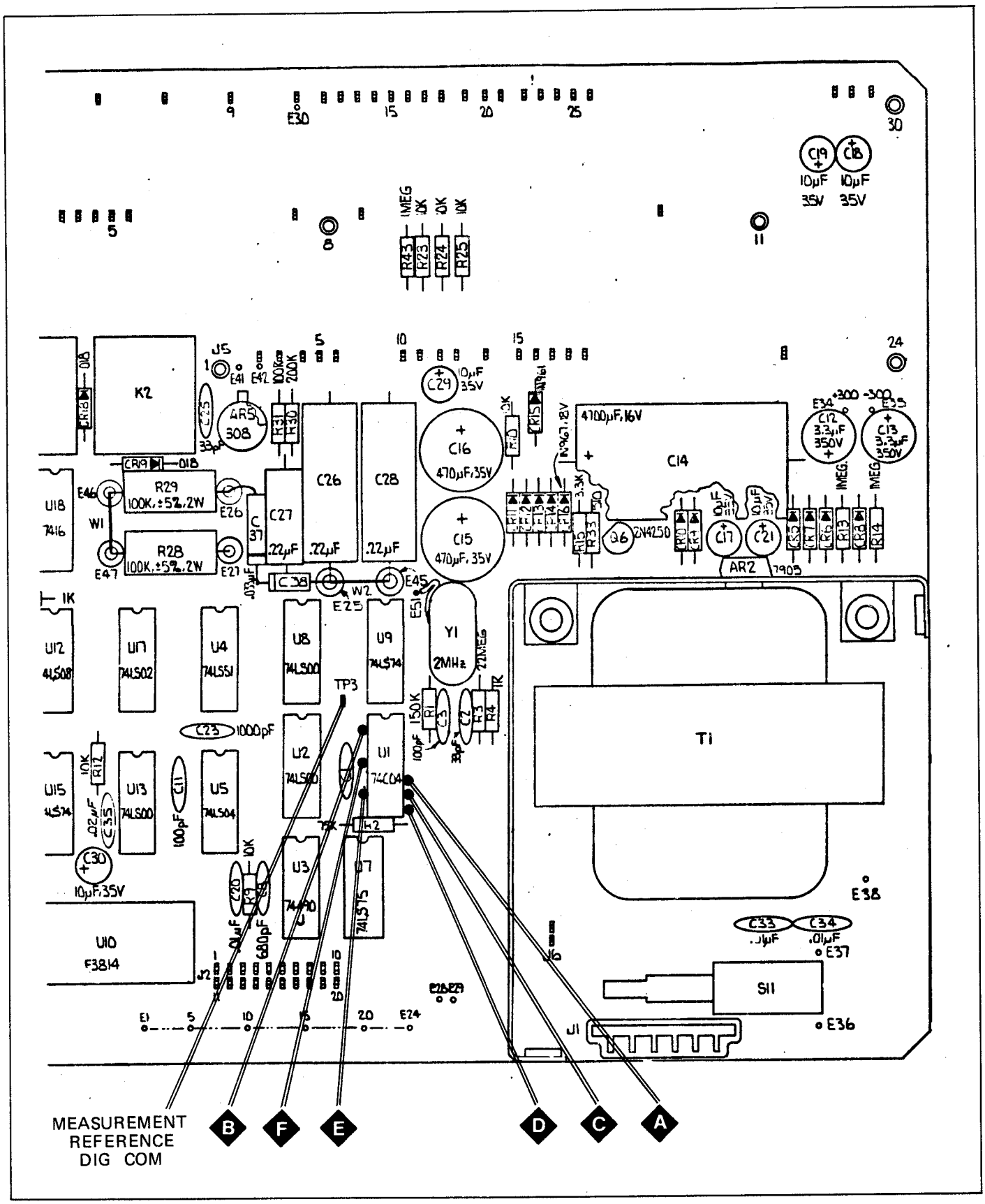


Figure 5.19 - Main PCB, Oscillator/Clock & MUX Oscillator Test Point Locations

Table 5.14 - Main PCB, Range/Function & Relay Logic Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .1 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper	ROM Inputs/Outputs	U21	1	Figure 5.23	NOTE: All measurements are referenced to TP3 (DIG COM)
Range: 1	ROM Inputs/Outputs	U21			
Range: 10	ROM Inputs/Outputs	U21			
Range: 100	ROM Inputs/Outputs	U21			
Range: 1000	ROM Inputs/Outputs	U21			
Function: ACV	ROM Inputs/Outputs	U21	1	Figure 5.23	
Range: 100	ROM Inputs/Outputs	U21			
Range: 10	ROM Inputs/Outputs	U21			
Range: 1	ROM Inputs/Outputs	U21			
Function: KΩ	ROM Inputs/Outputs	U21	1	Figure 5.23	
Range: .1	ROM Inputs/Outputs	U21			
Range: 1	ROM Inputs/Outputs	U21			
Range: 10	ROM Inputs/Outputs	U21			
Range: 100	ROM Inputs/Outputs	U21			
Range: 1000	ROM Inputs/Outputs	U21			
Range: 10,000	ROM Inputs/Outputs	U21			

		MAIN PCB		DIGITIZER PCB			AC CONV. PCB			ISOLATOR GAIN	
FUNCTION	RANGE	K1	K2	K1	K2	K3	K1	K2	K3	X1	X10
DCV & RATIO	.1		■								■
	1		■							■	
	10				■					■	
	100									■	
	1000	■								■	
ACV	1									■	
	10				■		■			■	
	100							■		■	
	1000								■	■	
KΩ	.1		■			■					■
	1		■			■				■	
	10		■		■					■	
	100		■							■	
	1000	■	■							■	
	10,000	■	■	■						■	

■ ENERGIZED

Figure 5.20 - Range Relay Status Chart

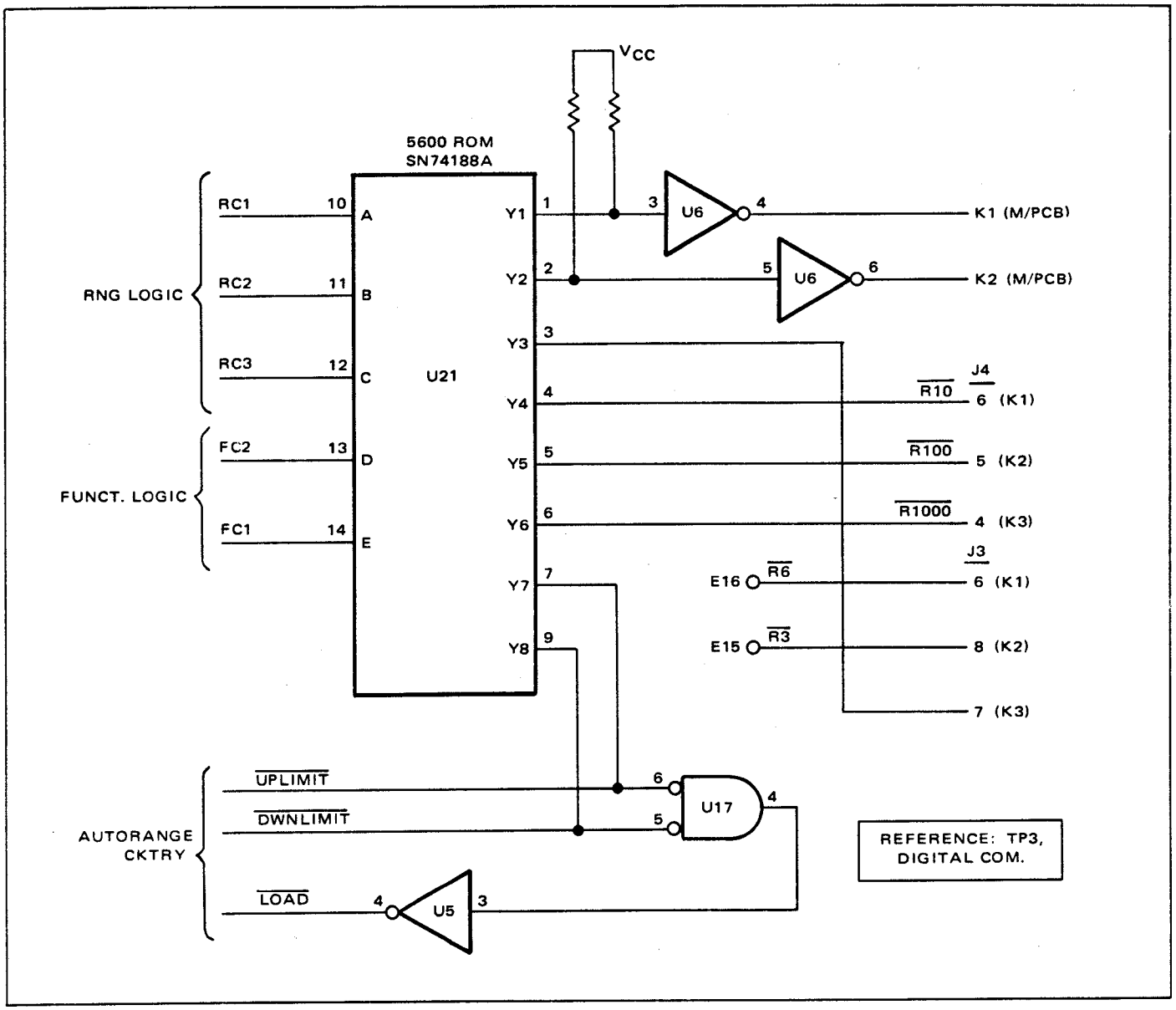


Figure 5.21 - Range and Function ROM Simplified Schematic

STATEMENTS

1. Inputs A(RC1), B(RC2), and C(RC3) are from the UP DOWN range counter to code range information. High levels (3.6V, REF: DIG COM) decode range.
2. Inputs D(FC2) and E(FC1) are from function logic/ switches to code function information. Low levels (0.15V, REF: DIG COM) decode function.
3. Outputs Y1 and Y2 are inverted to drive K1 and K2 on the main PCB for signal distribution for DCV and KΩ ranges. High outputs enable relays.
4. Outputs Y3, E16 ($\overline{R6}$, Display Decimal Code), and E15 ($\overline{R3}$, Display Decimal Code) drive K3, K1, and K2 respectively on the digitizer PCB to configure the HV buffer and/or attenuator for DCV and KΩ ranges. Low outputs enable relays.
5. Outputs Y4, Y5, and Y6 code range attenuation for the AC converter relays. Low outputs enable relays.
6. Outputs Y7 and Y8 decode $\overline{\text{UP LIMIT}}$ and $\overline{\text{DOWN LIMIT}}$ information for autoranging processes. Low outputs are range limits. If both outputs are low (power-up or illegal range), the up/down counter, U20, is set from range code 6 (hard-wired input code) when the $\overline{\text{load}}$ input goes low to protect signal input circuitry.

ROM IN

ROM OUT

DCV & RATIO X10

TYPICAL FOR ALL INPUTS	U21 PIN		.1	1	10	100	1000
RC1	A	10	L		L		L
RC2	B	11			L	L	
RC3	C	12	L	L			
FC2	D	13	H	H	H	H	H
FC1	E	14	H	H	H	H	H

U21 PIN		.1	1	10	100	1000	TYPICAL FOR ALL OUTPUTS
Y1	1	L	L	L	L		K1 – M/PCB
Y2	2			L	L	L	K2 – M/PCB
Y3	3	H	H	H	H	H	K3 – DIG
Y4	4	H	H	H	H	H	K1 – AC
Y5	5	H	H	H	H	H	K2 – AC
Y6	6	H	H	H	H	H	K3 – AC
Y7	7	H	H	H	H		$\overline{\text{UPLIMIT}}$
Y8	9		H	H	H	H	$\overline{\text{DWNLIMIT}}$
E16		H	H	H	H	H	K1 – DIG
E15		H	H		H	H	K2 – DIG

TRUE STATE — LOGIC LEVEL

= HIGH = H

= LOW = L

TYPICAL FOR ALL TABLES

a

ACV

U21 PIN			1	10	100	1000
A	10	*		L		L
B	11			L	L	
C	12		L			
D	13		H	H	H	H
E	14					

U21 PIN			1	10	100	1000
Y1	1	*	L	L	L	L
Y2	2		L	L	L	L
Y3	3		H	H	H	H
Y4	4		H		H	H
Y5	5		H	H		H
Y6	6		H	H	H	
Y7	7		H	H	H	
Y8	9			H	H	H
E16			H	H	H	H
E15			H		H	H

b

KΩ

U21 PIN		.1	1	10	100	1000	10,000
A	10	L		L		L	
B	11			L	L		
C	12	L	L				
D	13						
E	14	H	H	H	H	H	H

* THESE RANGES DO NOT EXIST

U21 PIN		.1	1	10	100	1000	10,000
Y1	1	L	L	L	L		
Y2	2						
Y3	3			H	H	H	H
Y4	4	H	H	H	H	H	H
Y5	5	H	H	H	H	H	H
Y6	6	H	H	H	H	H	H
Y7	7	H	H	H	H	H	
Y8	9		H	H	H	H	H
E16		H	H	H	H	H	
E15		H	H		H	H	H

c

Figure 5.22 - Relay Logic Level Performance Standard

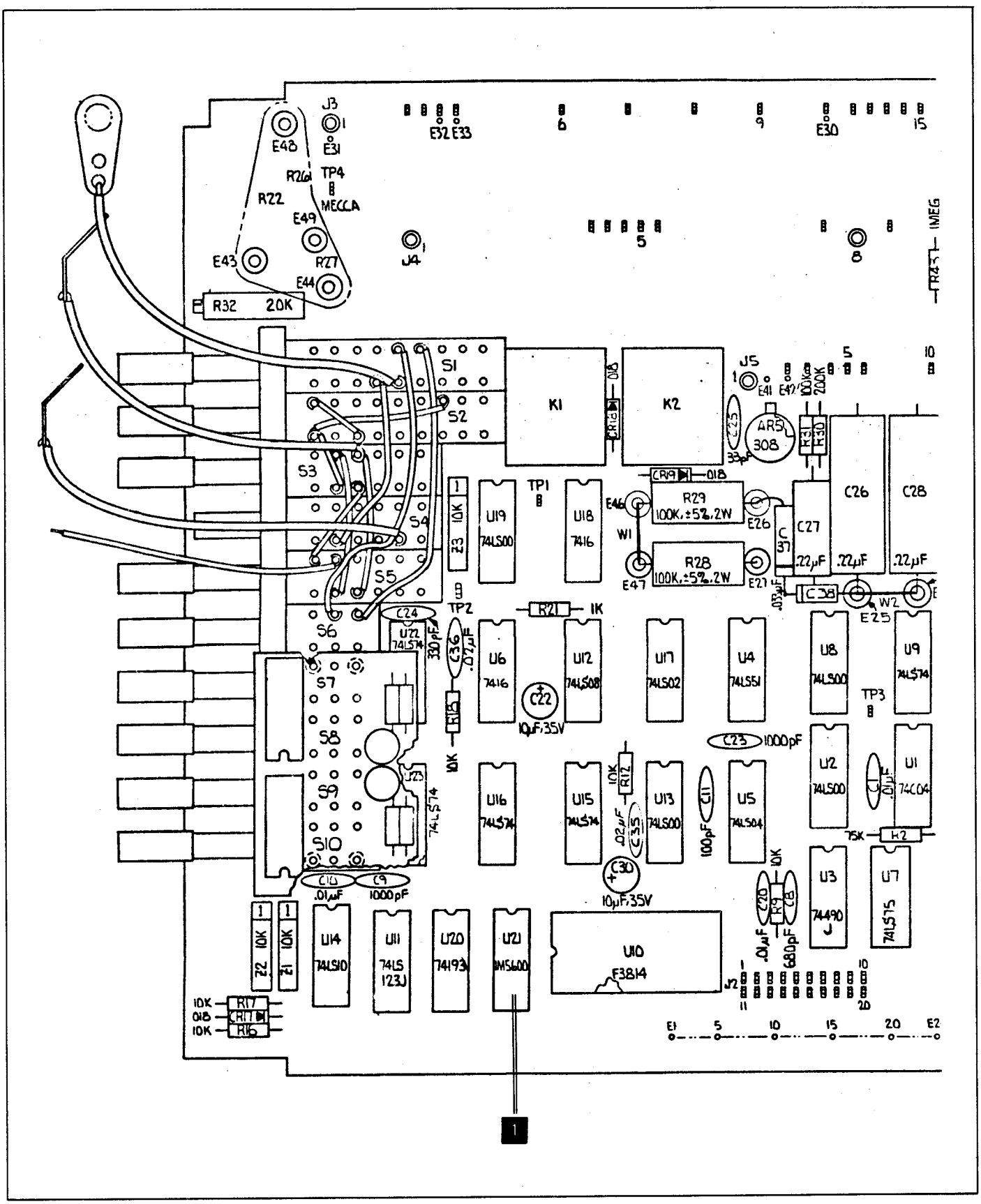


Figure 5.23 - Main PCB, Range/Function & Relay Logic Test Point Locations

Table 5.15 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: AUTO Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP3 (DIG COM) NOTE: External trigger oscilloscope at TP1 (SID)
	Counter Output Q_{e1}	U10-18/U13-5	G	Figure 5.24	Waveform 1
	Counter Output Q_{e2}	U10-16/U13-4	H	Figure 5.24	Waveform 2
	$\overline{\text{Signal Integrate}}$	U13-6	I	Figure 5.24	Waveform 3
	$\overline{\text{Reset}}$	U13-11	J	Figure 5.24	Waveform 4
Remove jumper and connect to a DC standard set at +.100000V	$\overline{\text{Null Detect}}$	TP2	K	Figure 5.24	Waveform 5_1
Reverse Signal Polarity	$\overline{\text{Null Detect}}$	TP2	K	Figure 5.24	Waveform 5_2
Reverse Signal Polarity	+ND F/F Output	U14-1	L	Figure 5.24	Waveform 6
	–ND F/F Output	U14-2	M	Figure 5.24	Waveform 7
	Internal Reset	U14-12	N	Figure 5.24	Waveform 8
	Signal Integrate	U13-3	O	Figure 5.24	Waveform 9
	Reference Integrate Enable	U17-13	P	Figure 5.24	Waveform 10
	– Reference Switch Drive	U18-6	Q	Figure 5.24	Waveform 11
	Freq/10 Switch Output	U4-6	R	Figure 5.24	Waveform 12
	Prescale Counter "A" Output	U3-3	S	Figure 5.24	Waveform 13
	Prescale Counter "D" Output	U3-7	T	Figure 5.24	Waveform 14
	Counter Control F/F "D" Input	U9-2	U	Figure 5.24	Waveform 15

Table 5.15 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test continued

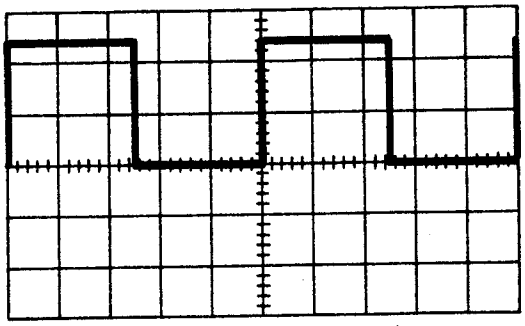
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Counter Control F/F Clock Input	U9-3	V	Figure 5.24	Waveform 16
	Counter Control F/F Q Output	U9-6	W	Figure 5.24	Waveform 17
	One-Shot "A" Q Output	U11-4	X	Figure 5.24	Waveform 18
	One-Shot "B" Q Output	U11-12	Y	Figure 5.24	Waveform 19
Remove DC standard voltage input					

WAVEFORMS FOR TABLE 5.15

1 (NO.)

Q_{e1}

U10-18



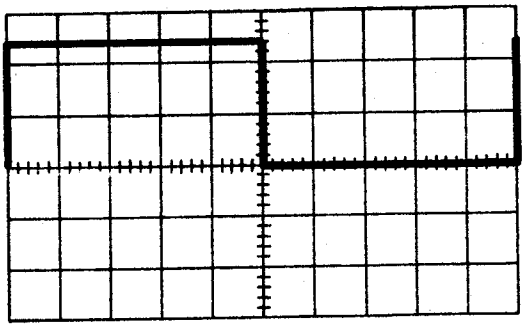
2.0 (V/DIV)

20 mS (S/DIV)

2 (NO.)

Q_{e2}

U10-16



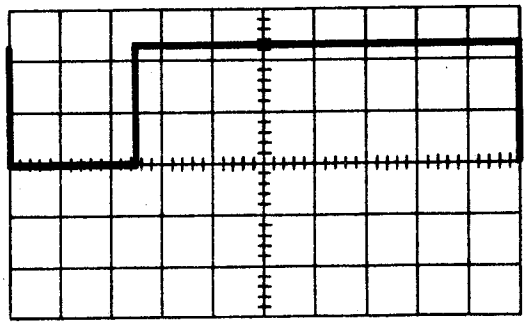
2.0 (V/DIV)

20 mS (S/DIV)

3 (NO.)

$\overline{\text{SIGNAL INTEGRATE}}$

U13-6



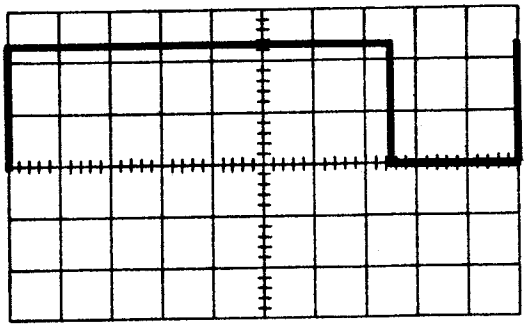
2.0 (V/DIV)

20 mS (S/DIV)

4 (NO.)

$\overline{\text{RESET}}$

U13-11



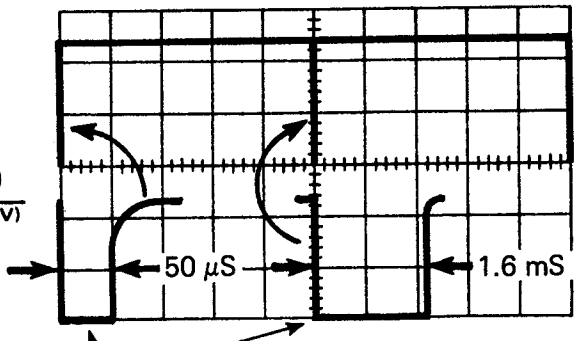
2.0 (V/DIV)

20 mS (S/DIV)

5_1 (NO.)

$\overline{\text{NULL DETECT}}$ (+ POL)

TP2



2.0 (V/DIV)

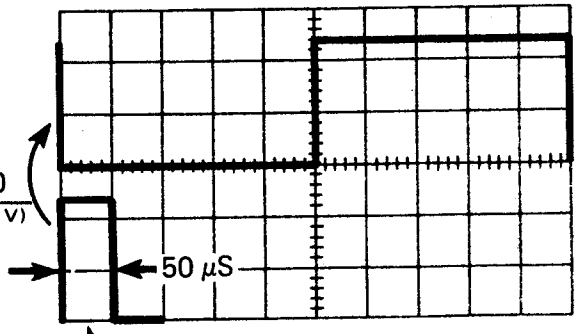
EXPANDED VIEWS

20 mS (S/DIV)

5_2 (NO.)

$\overline{\text{NULL DETECT}}$ (– POL)

TP2



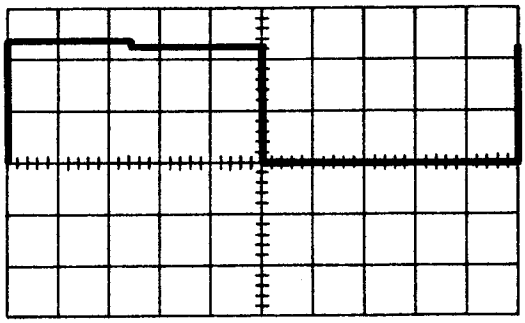
2.0 (V/DIV)

EXPANDED VIEW

20 mS (S/DIV)

6 (NO.) + NULL DETECT F/F

U14-1

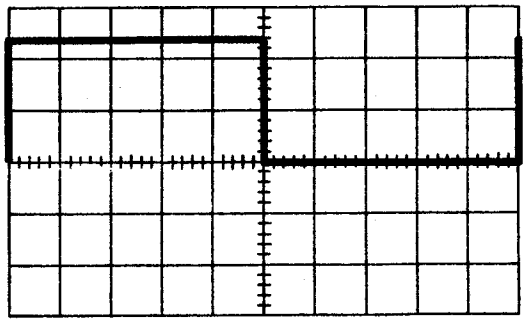


2.0 (V/DIV)

20 mS (S/DIV)

7 (NO.) – NULL DETECT F/F

U14-2

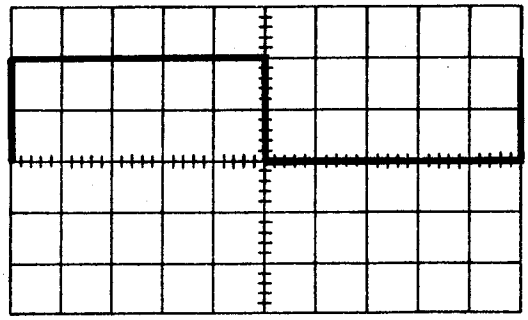


2.0 (V/DIV)

20 mS (S/DIV)

8 (NO.) INTERNAL RESET

U14-12

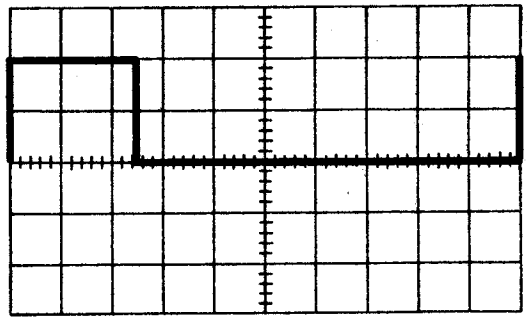


2.0 (V/DIV)

20 mS (S/DIV)

9 (NO.) SIGNAL INTEGRATE

U13-3

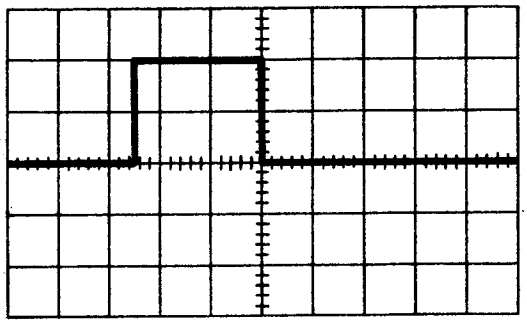


2.0 (V/DIV)

20 mS (S/DIV)

10 (NO.) REFERENCE INTEGRATE ENABLE

U17-13

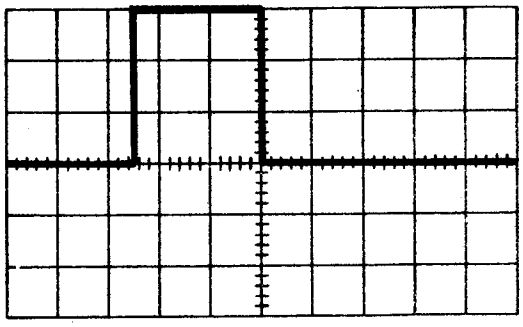


2.0 (V/DIV)

20 mS (S/DIV)

11 (NO.) – REFERENCE INTEGRATE (– RD)

U18-6



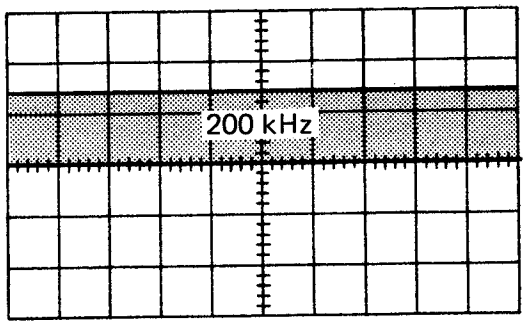
5.0 (V/DIV)

20 mS (S/DIV)

WAVEFORMS FOR TABLE 5.15 continued

12 (NO.) FQ/10 SW OUTPUT

U4-6

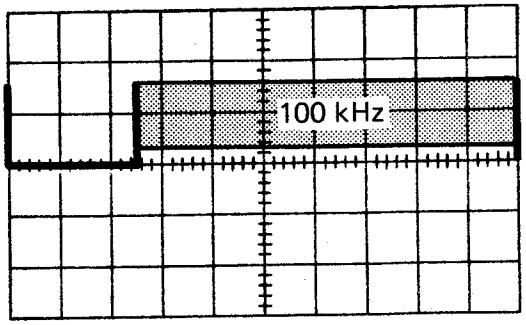


2.0 (V/DIV)

20 mS (S/DIV)

13 (NO.) PRESCALE GATE "A" OUTPUT

U3-3

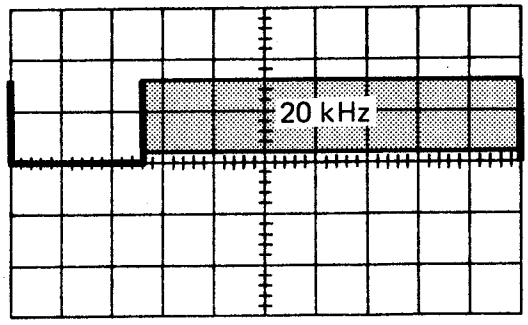


2.0 (V/DIV)

20 mS (S/DIV)

14 (NO.) PRESCALE CONTROL "D" OUTPUT

U3-7

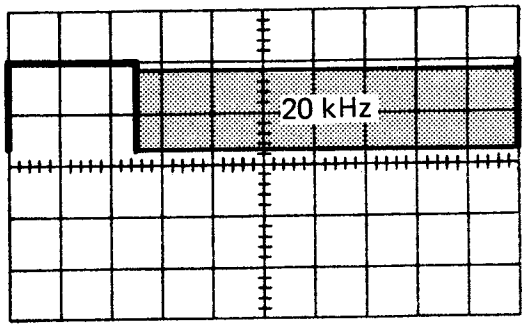


2.0 (V/DIV)

20 mS (S/DIV)

15 (NO.) COUNTER CONTROL F/F "D" INPUT

U9-2

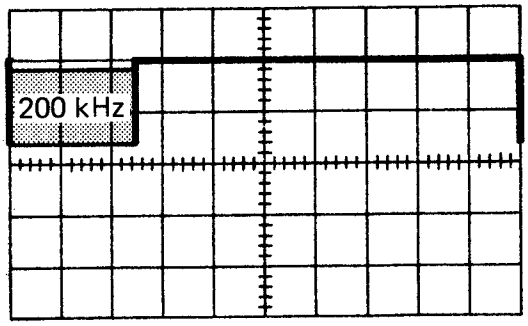


2.0 (V/DIV)

20 mS (S/DIV)

16 (NO.) COUNTER CONTROL F/F CLOCK INPUT

U9-3

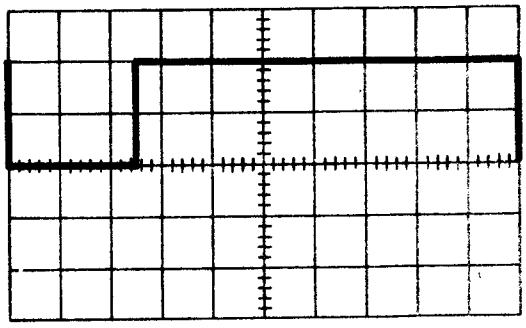


2.0V (V/DIV)

20 mS (S/DIV)

17 (NO.) COUNTER CONTROL F/F $\overline{Q}$ OUTPUT

U9-6



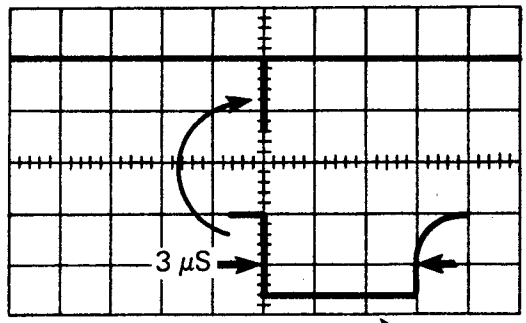
2.0V (V/DIV)

20 mS (S/DIV)

WAVEFORMS FOR TABLE 5.15 continued

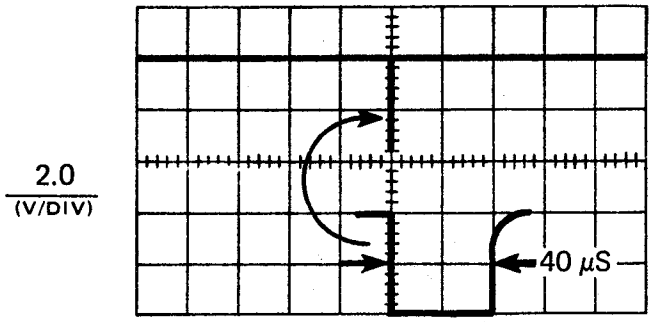
18 (NO.) ONE/SHOT "A" $\overline{Q}$ OUTPUT

U11-4



19 (NO.) ONE/SHOT "B" $\overline{Q}$ OUTPUT

U11-12



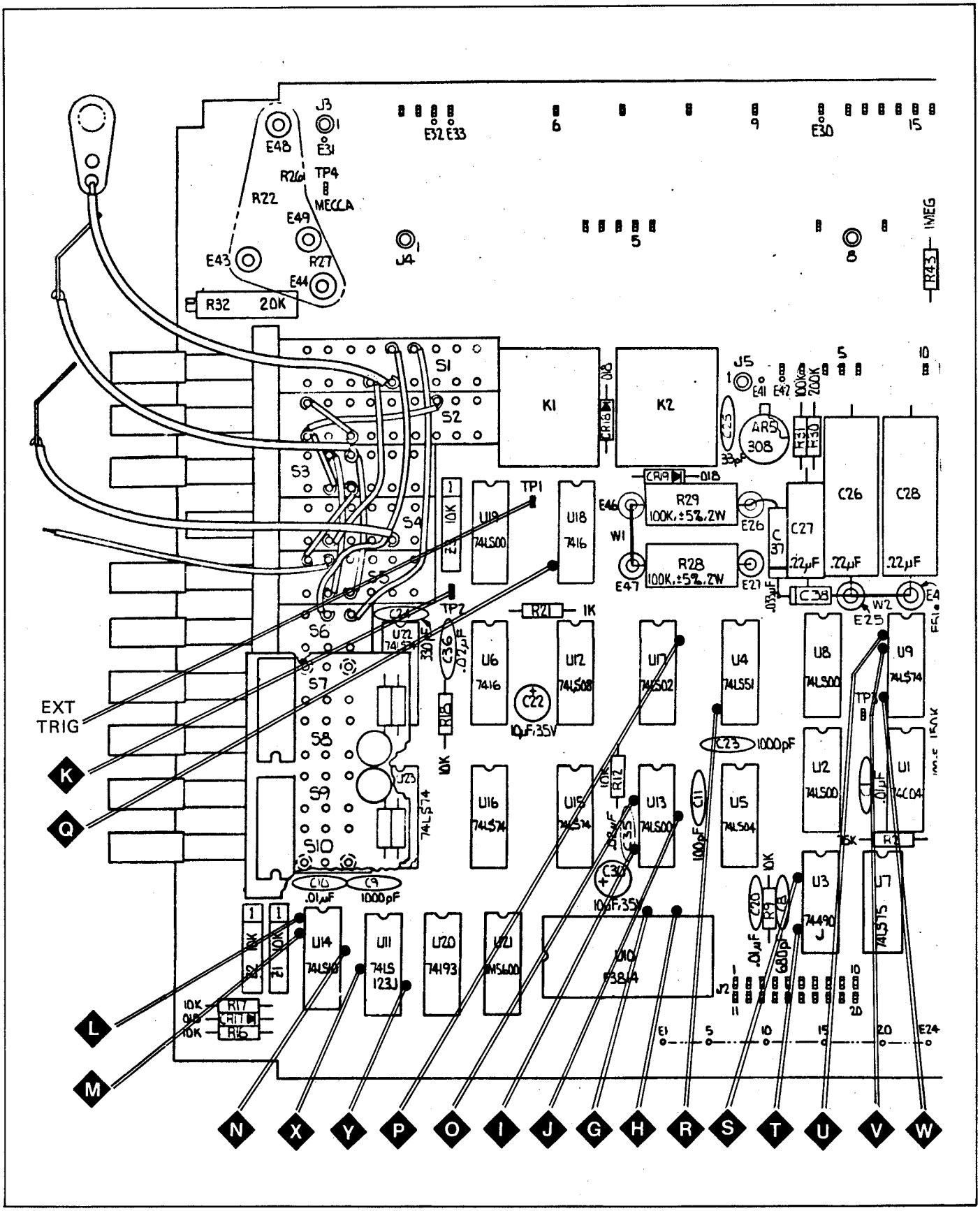


Figure 5.24 - Main PCB, Counter & Timing/Control Logic Test Point Locations

Table 5.16 - Main PCB, Measurement Filter Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 1 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA)
					NOTE: Signal or function generator having a DC component must be decoupled with a .01 μF cap
	Filter Amp – Input	R30	2	Figure 5.25	±0.0001V DC
	Filter Amp Output	R31	3	Figure 5.25	±0.0001V DC
Remove jumper. Connect input terminals to a function generator set to 10 kHz @ 2V p-p measured at E27	Decoupled Isolator Input	E26	Z	Figure 5.25	250 mV p-p (18 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	50 μV p-p (92 dB)
Filter: OUT Generator set to 2V p-p @ 1 kHz measured @ E27	Decoupled Isolator Input	E26	Z	Figure 5.25	900 mV p-p (7 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	20 μV p-p (100 dB)
Filter: OUT Generator set to 2V p-p @ 100 Hz measured @ E27	Decoupled Isolator Input	E26	Z	Figure 5.25	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	50 μV p-p (92 dB)
Filter: OUT Generator set to 2V p-p @ 60 Hz measured @ E27	Decoupled Isolator Input	E26	Z	Figure 5.25	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	1.5 mV p-p (62 dB)

Table 5.16 - Main PCB, Measurement Filter Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Filter: OUT Generator set to 2V p-p @ 50 Hz measured @ E27	Decoupled Isolator Input	E26	Z	Figure 5.25	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	2 mV p-p (60 dB)
Filter: OUT Generator set to 2V p-p @ 40 Hz measured @ E27	Decoupled Isolator Input	E26	Z	Figure 5.25	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	4 mV p-p (54 dB)
Filter: OUT Generator set to 2V p-p @ 20 Hz measured @ E27	Decoupled Isolator Input	E26	Z	Figure 5.25	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	Z	Figure 5.25	20 mV p-p (40 dB)

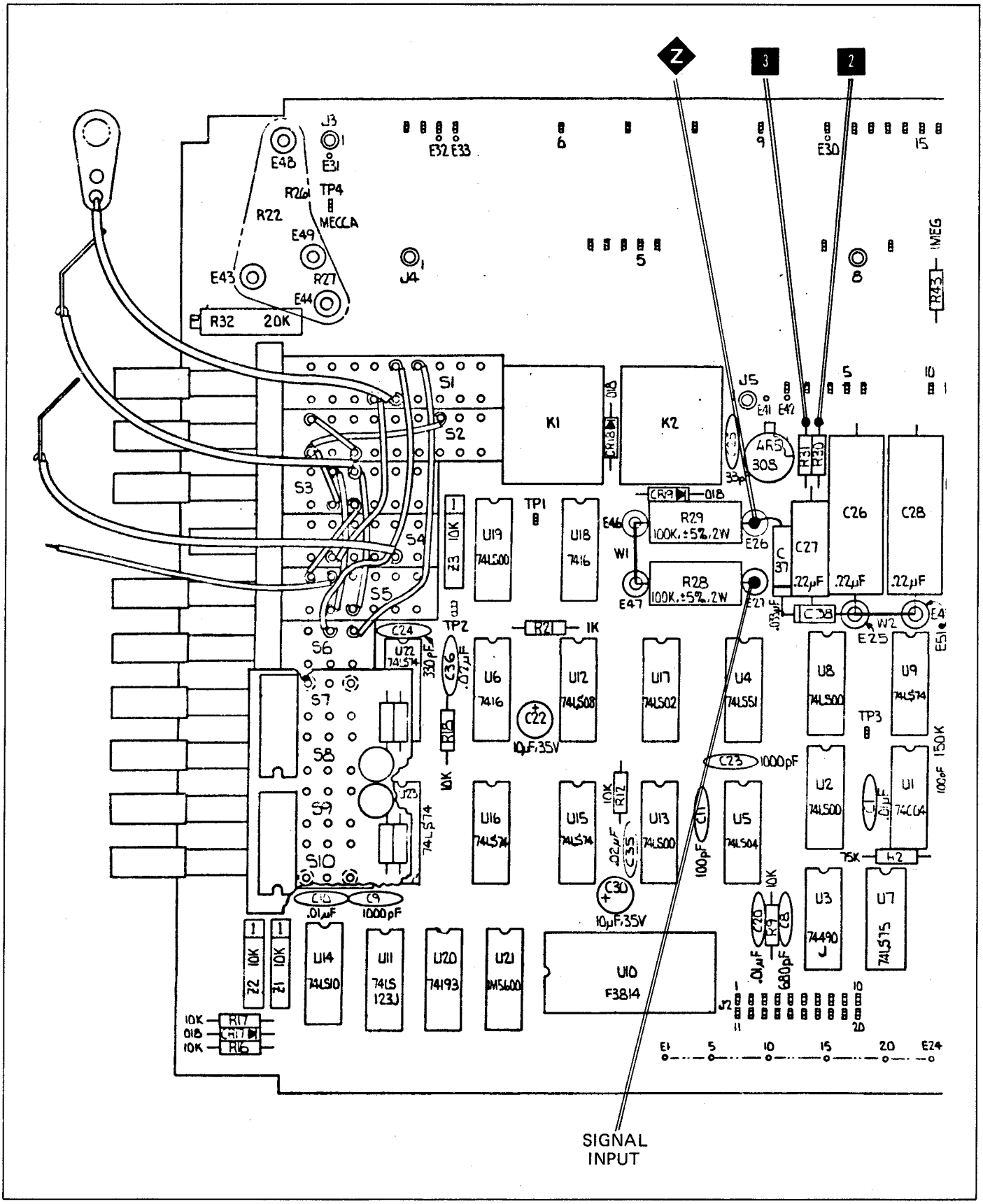


Figure 5.25 - Main PCB, Measurement Filter Test Point Locations

Table 5.17 - Display PCB, Subassembly Performance Test

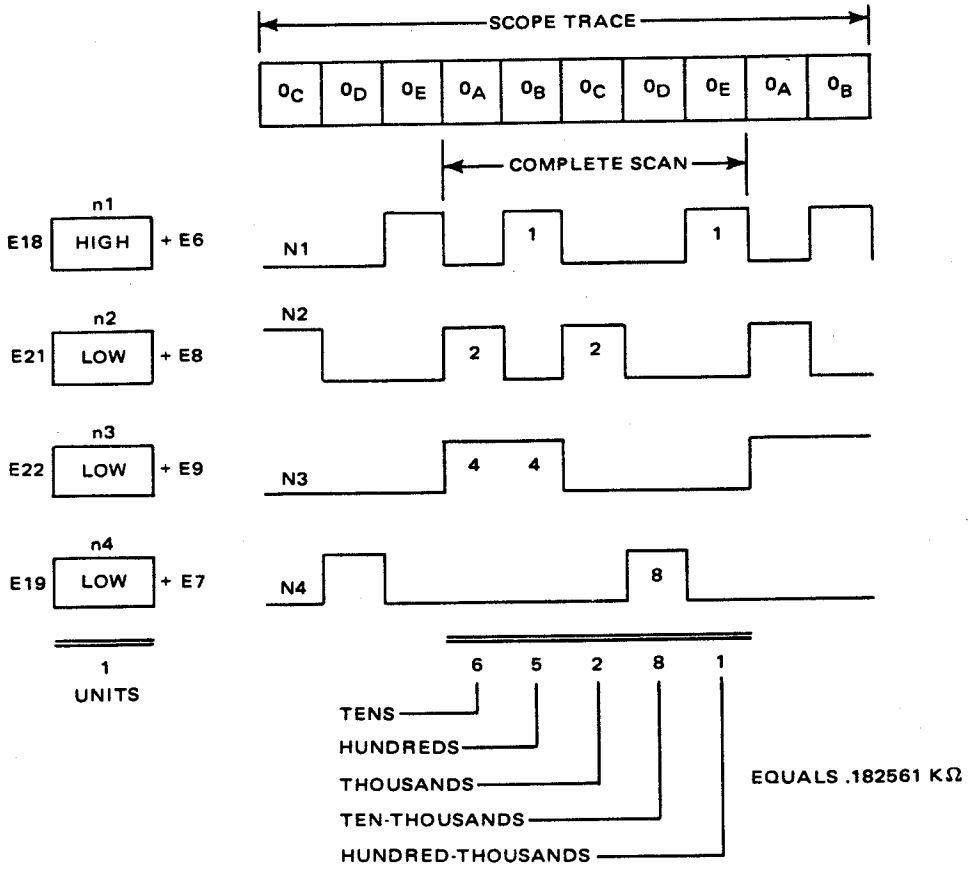
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: KΩ Range: .1 (manual) Filter: OUT Input Terminals: J101/ J103 connected with a copper jumper to J102/ J104. (Guard connected to J102/J104)					NOTE: All measurements are referenced to TP3 (DIG COM) Main PCB
					NOTE: Ext Trig for MUX output drive is J2-3, Main PCB
					NOTE: Decimal input logic levels: High = +3.7V DC Low = +0.17V DC
	RC1	E14	1	Figure 5.26	Logic Low — LED 2 Decimal Point
	RC2	E13	2	Figure 5.26	Logic High — LED 2 Decimal Point
	RC3	E12	3	Figure 5.26	Logic Low — LED 2 Decimal Point
Range: 1 (manual)	RC1	E14	1	Figure 5.26	Logic High — LED 3 Decimal Point
	RC2	E13	2	Figure 5.26	Logic High — LED 3 Decimal Point
	RC3	E12	3	Figure 5.26	Logic Low — LED 3 Decimal Point
Range: 10 (manual)	RC1	E14	1	Figure 5.26	Logic Low — LED 4 Decimal Point
	RC2	E13	2	Figure 5.26	Logic Low — LED 4 Decimal Point
	RC3	E12	3	Figure 5.26	Logic High — LED 4 Decimal Point
Range: 100 (manual)	RC1	E14	1	Figure 5.26	Logic High — LED 5 Decimal Point
	RC2	E13	2	Figure 5.26	Logic Low — LED 5 Decimal Point
	RC3	E12	3	Figure 5.26	Logic High — LED 5 Decimal Point
Range: 1000 (manual)	RC1	E14	1	Figure 5.26	Logic Low — LED 6 Decimal Point
	RC2	E13	2	Figure 5.26	Logic High — LED 6 Decimal Point
	RC3	E12	3	Figure 5.26	Logic High — LED 6 Decimal Point

Table 5.17 - Display PCB, Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Range: 10,000 (manual)	RC1	E14	1	Figure 5.26	Logic High — LED 7 Decimal Point
	RC2	E13	2	Figure 5.26	High — LED 7 Decimal Point
	RC3	E12	3	Figure 5.26	High — LED 7 Decimal Point
	O_D	E1	A	Figure 5.26	Waveform 1
	O_C (Ext Trig)	E2	B	Figure 5.26	Waveform 2
	O_B	E3	C	Figure 5.26	Waveform 3
	O_E	E4	D	Figure 5.26	Waveform 4
	O_A	E5	E	Figure 5.26	Waveform 5
	LED 3 DR	Q2 Collector	F	Figure 5.26	Waveform 6
	LED 4 DR	Q3 Collector	G	Figure 5.26	Waveform 7
	LED 5 DR	Q4 Collector	H	Figure 5.26	Waveform 8
	LED 2 DR	Q1 Collector	I	Figure 5.26	Waveform 9
	LED 6/7 DR	Q5/Q6 Collector	J	Figure 5.26	Waveform 10
Remove Short from Input Terminals	$\overline{\text{Blank}}$	E20	K	Figure 5.26	Waveform 11 Display flashes 200000
Connect Input Terminals with a copper jumper. Enable Lite Test Switch, S7	$\overline{\text{LED Segment Test}}$			Figure 5.26	All Decade Segments illuminate 8 8 8 8 8 8
Remove Short from Input Terminals. Connect input terminal to a resistance value. Example: .182561 (KΩ) Ext Trig Scope @ J2-3, Main PCB	N_1 Counter Output	E6	L	Figure 5.26	Waveform 12
	N_2 Counter Output	E8	M	Figure 5.26	Waveform 13
	N_3 Counter Output	E9	N	Figure 5.26	Waveform 14
	N_4 Counter Output	E7	O	Figure 5.26	Waveform 15

Table 5.17 - Display PCB, Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Ext Trig Scope @ TP1, Main PCB	n1 LSD Counter Output	E18	4	Figure 5.26	Logic High
	n2 LSD Counter Output	E21	5	Figure 5.26	Logic Low
	n3 LSD Counter Output	E22	6	Figure 5.26	Logic Low
	n4 LSD Counter Output	E19	7	Figure 5.26	Logic Low
Function: DCV Range: AUTO Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected to a +1V source	$\overline{\text{Plus Polarity}}$	E10	8	Figure 5.26	Logic Low
Change Input to −1V Source	$\overline{\text{Minus Polarity}}$	E11	9	Figure 5.26	Logic Low
Disconnect Input Scope and Ext Trig Cables					

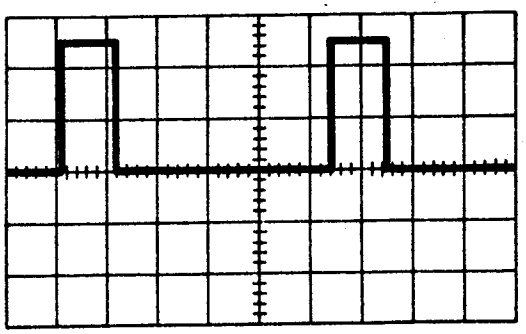


WAVEFORMS FOR TABLE 5.17

1 (NO.)

O_D MUX DR

E1



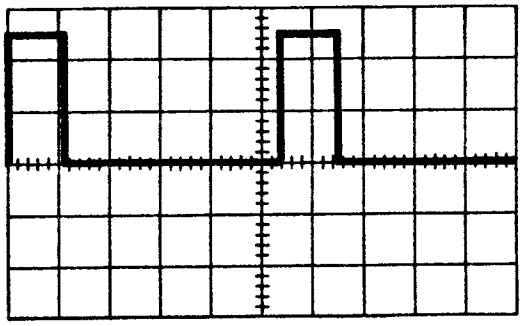
2.0 (V/DIV)

2 mS (S/DIV)

2 (NO.)

O_C MUX DR (EXT TRIG)

E2



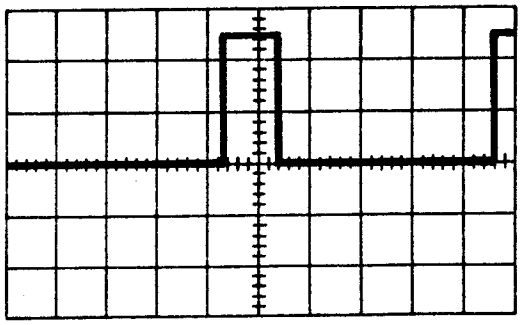
2.0 (V/DIV)

2 mS (S/DIV)

3 (NO.)

O_B MUX DR

E3



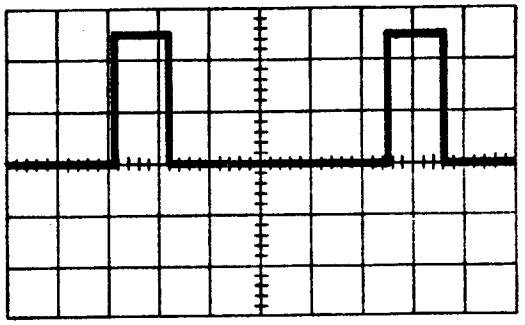
2.0 (V/DIV)

2 mS (S/DIV)

4 (NO.)

O_E MUX DR

E4



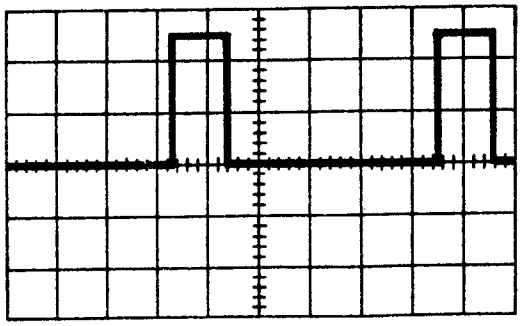
2.0 (V/DIV)

2 mS (S/DIV)

5 (NO.)

O_A MUX DR

E5



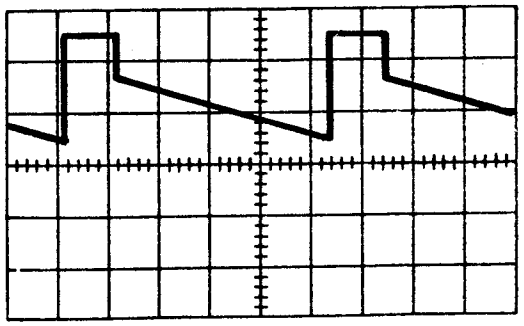
2.0 (V/DIV)

2 mS (S/DIV)

6 (NO.)

LED 3 DR

Q2 COLLECTOR

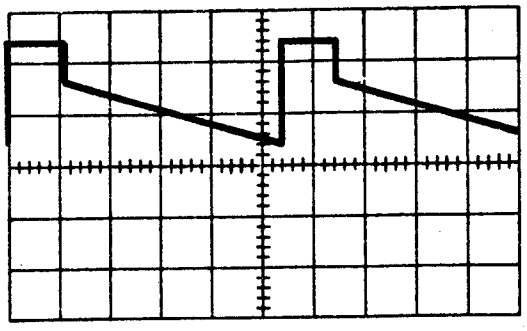


2.0 (V/DIV)

2 mS (S/DIV)

WAVEFORMS FOR TABLE 5.17 continued

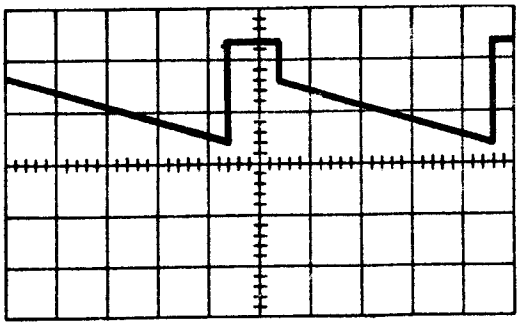
7 (NO.) LED 4 DR
Q3 COLLECTOR



2.0 (V/DIV)

2 mS (S/DIV)

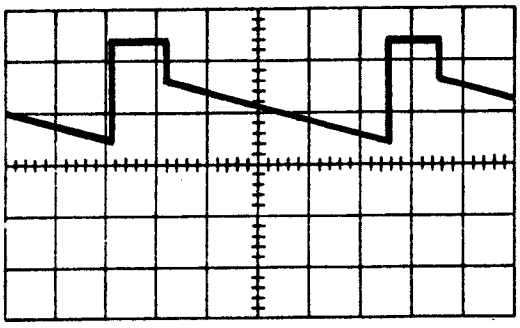
8 (NO.) LED 5 DR
Q4 COLLECTOR



2.0 (V/DIV)

2 mS (S/DIV)

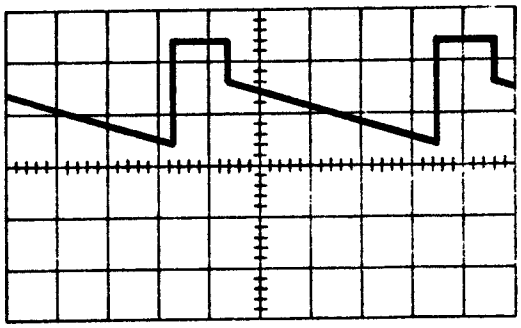
9 (NO.) LED 2 DR
Q1 COLLECTOR



2.0 (V/DIV)

2 mS (S/DIV)

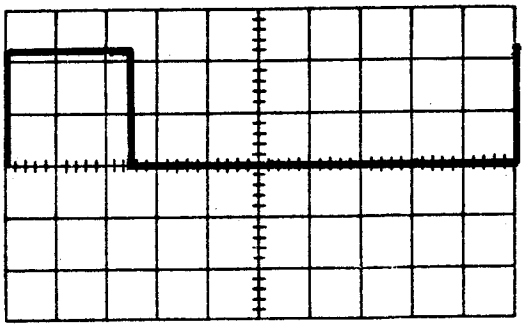
10 (NO.) LED 617 DR
Q5/6 COLLECTORS



2.0 (V/DIV)

2 mS (S/DIV)

11 (NO.) $\overline{\text{BLANK}}$
E20

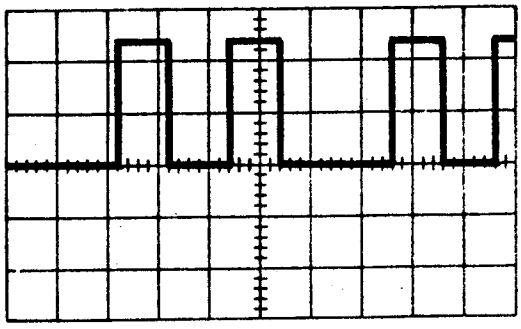


2.0 (V/DIV)

20 mS (S/DIV)

EXT TRIG @ TP1 (SID) MAIN PCB

12 (NO.) N_1 COUNTER OUTPUT
E6



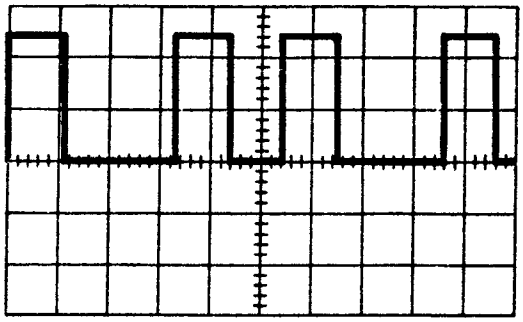
2.0 (V/DIV)

2 mS (S/DIV)

EXT TRIG @ J2-3, MAIN PCB

WAVEFORMS FOR TABLE 5.17 continued

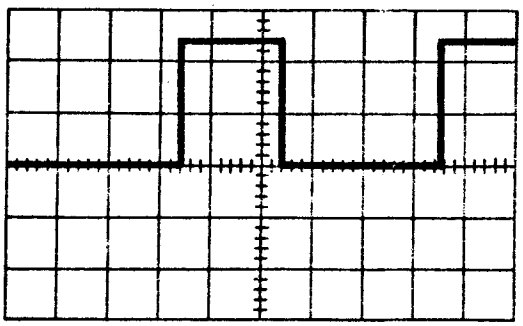
13 (NO.) N_2 COUNTER OUTPUT
E8



2.0 (V/DIV)

2 mS (S/DIV)

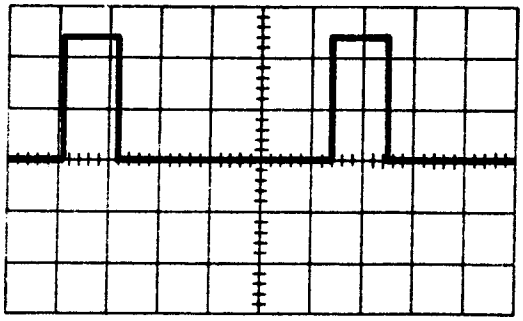
14 (NO.) N_3 COUNTER OUTPUT
E9



2.0 (V/DIV)

2 mS (S/DIV)

15 (NO.) N_4 COUNTER OUTPUT
E7



2.0 (V/DIV)

2 mS (S/DIV)

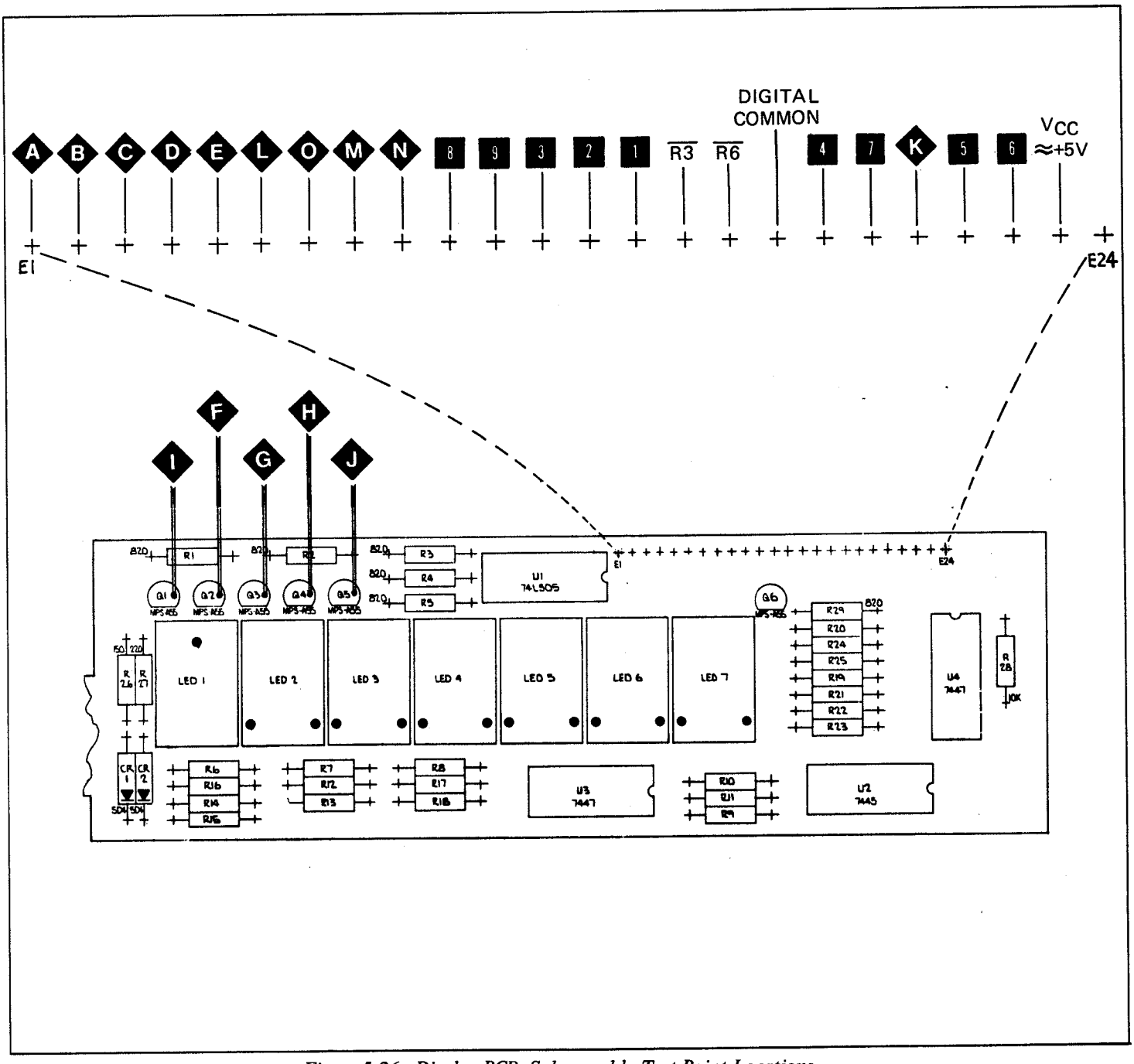
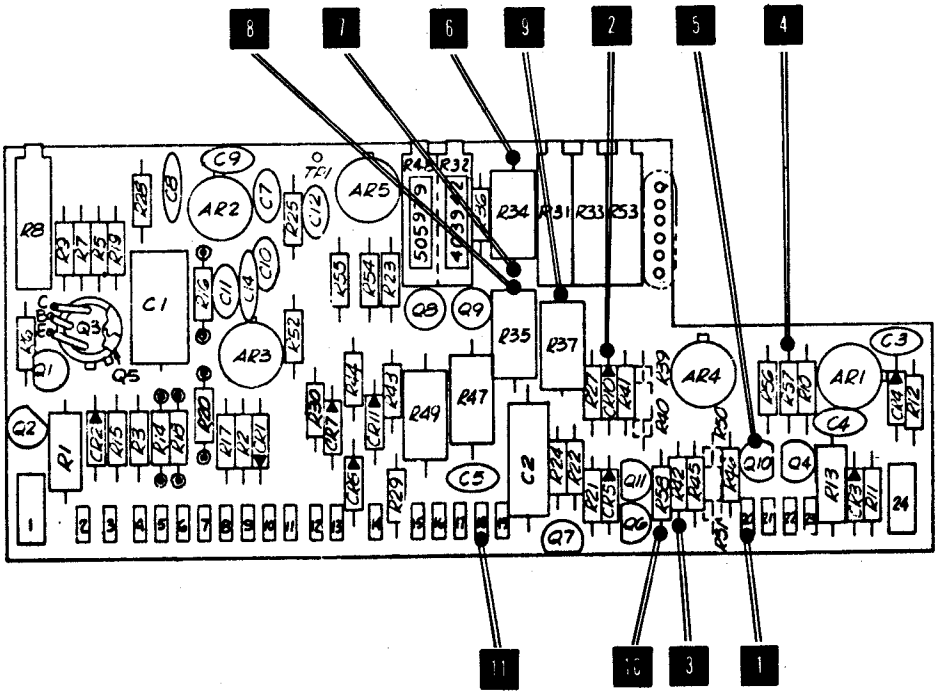


Figure 5.26 - Display PCB, Subassembly Test Point Locations

Table 5.18 - Reference Isolator PCB, Internal Reference Generator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 1, Manual Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Reference Zener Diodes (CR10) can vary from +6.2V to +6.4V. Performance standard voltages are measured values on a sample DMM
NOTE: The AC Converter must be removed to gain access to test points	Reference Common	P5-20	1	Figure 5.27	+0.000156V DC
	Reference Zener	CR10 (Cathode)	2	Figure 5.27	+6.3326V DC
	Op Amp + In	R42	3	Figure 5.27	+6.1924V DC
	Op Amp Output	R57	4	Figure 5.27	+10.6387V DC
	Reference Gen. Output	Q10 (Emitter)	5	Figure 5.27	+10.0022V DC
	Bridge Gain Resistor	R34	6	Figure 5.27	+9.9918V DC
	Op Amp – In	R34	7	Figure 5.27	+6.1998V DC
	Bridge Gain Resistor	R35	8	Figure 5.27	+0.99620V DC
	Bridge Gain Resistor	R37	9	Figure 5.27	+0.99516V DC
	Current Sink Bias	R58	10	Figure 5.27	–0.63020V DC
	+1V Reference Out	P5-18	11	Figure 5.27	+0.99583V DC



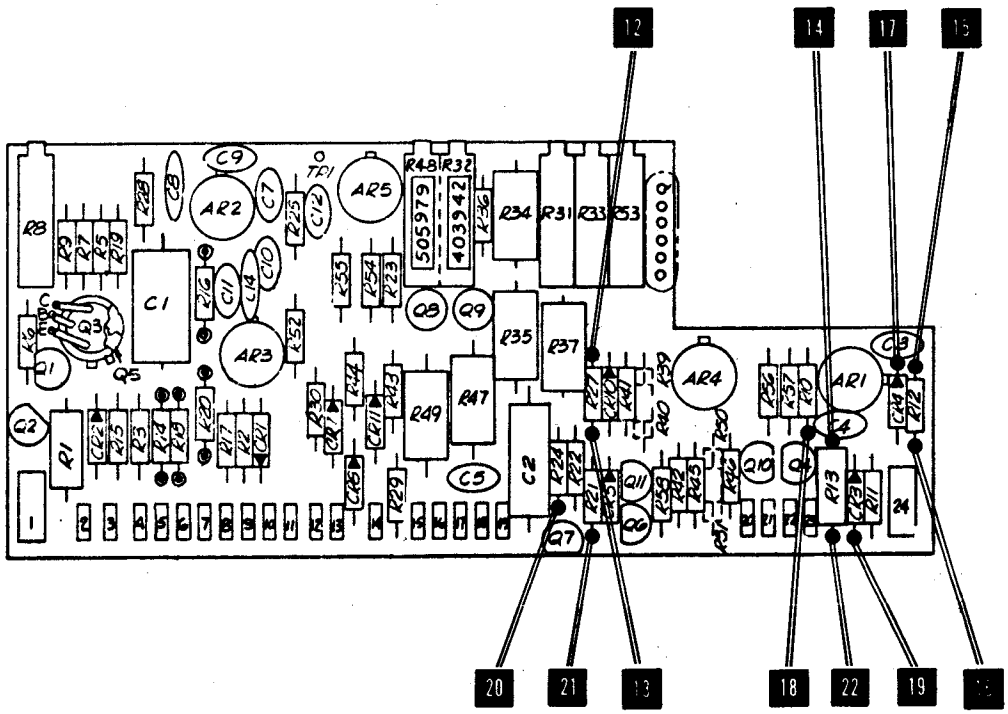
Typical DC Voltages for Reference Generator
Referenced to TP4 (MECCA) on Main PCB

1	+0.000156V DC	7	+6.1998V DC
2	+6.3326V DC	8	+0.99620V DC
3	+6.1924V DC	9	+0.99516V DC
4	+10.6387V DC	10	–0.63020V DC
5	+10.0022V DC	11	+0.99583V DC
6	+9.9918V DC		

Figure 5.27 - DC Reference Generator Test Point Locations

Table 5.19 - Reference Isolator PCB, KΩ Reference Generator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 1, Manual Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA) on Main PCB NOTE: DC reference generator circuit must be operational to obtain test results for the KΩ reference generator
NOTE: The AC Converter must be removed to gain access to test points	+10V DC Reference Generator Output	R27	12	Figure 5.28	+9.9986V DC
	KΩ Ref Op Amp – In	R27	13	Figure 5.28	+8.2630V DC
	KΩ Ref Op Amp + In	R13	14	Figure 5.28	+9.9985V DC
	KΩ Ref Op Amp Output	R12	15	Figure 5.28	+17.276V DC
	KΩ Ref Op Amp Decoupled Output	R12	16	Figure 5.28	+17.087V DC
	KΩ Over Voltage Protection Bias	CR4 (Cathode)	17	Figure 5.28	+17.633V DC
	KΩ Over Voltage Protection Bias	R10	18	Figure 5.28	+17.854V DC
	KΩ Over Voltage Protection Bias	CR3 (Anode)	19	Figure 5.28	+10.0525V DC
	KΩ Open Terminal Clamp Bias	R24	20	Figure 5.28	+17.009V DC
	KΩ Open Terminal Clamp Bias	R21	21	Figure 5.28	–2.5707V DC
	+10V KΩ Ref Voltage Output	R13	22	Figure 5.28	+9.9987V DC



Typical Voltages for KΩ Reference Generator Circuit
Referenced to TP4 (MECCA) on Main PCB

12	+9.9986V DC	18	+17.854V DC
13	+8.2630V DC	19	+10.5025V DC
14	+9.9985V DC	20	+17.009V DC
15	+17.276V DC	21	–2.5707V DC
16	+17.087V DC	22	+9.9987V DC
17	+17.633V DC		

Figure 5.28 - KΩ Reference Generator Test Point Locations

Table 5.20 - Reference Isolator PCB, Isolator/Bootstrap Subassembly Performance Test

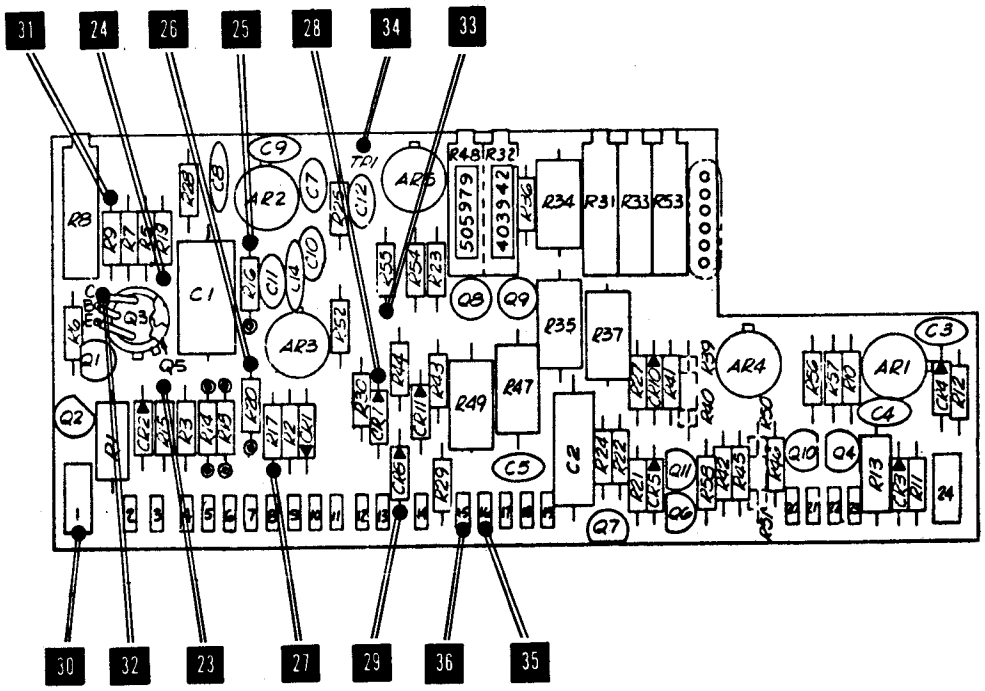
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 1, Manual Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper NOTE: The AC Converter must be removed to gain access to test points					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
	Isolator Op Amp – In	R15	23	Figure 5.29	+1.34425V DC
	Isolator Op Amp + In	R19	24	Figure 5.29	+1.34386V DC
	1st Stage Emitter Bias (Signal)	R16	25	Figure 5.29	–0.44451V DC
	1st Stage Emitter Bias (Reference)	R20	26	Figure 5.29	–0.44475V DC
	1st Stage Emitter Bias	R17	27	Figure 5.29	–0.44515V DC
	+ Bootstrap Voltage	CR7 (Cathode)	28	Figure 5.29	+4.9464V DC
	– Bootstrap Voltage	CR8 (Anode)	29	Figure 5.29	–5.1634V DC
	Bootstrap Common	J5-1	30	Figure 5.29	–.004212V DC
	Input Bias Network Divider Bias	R9	31	Figure 5.29	+0.32148V DC
	Input Bias Network Diode Drop	Q3 (Collector)	32	Figure 5.29	+0.113454V DC
	Current Sink Op Amp Output	R55	33	Figure 5.29	–0.005905V DC
	Isolator Output	TP1	34	Figure 5.29	–0.000002V DC

Table 5.20 - Reference Isolator PCB, Isolator/Bootstrap Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Remove copper jumper Range: .1, Manual Connect the Input Terminals to a DC standard set to +.100000V DC	Isolator Op Amp – In	R15	23	Figure 5.29	+1.44185V DC
	Isolator Op Amp + In	R19	24	Figure 5.29	+1.44235V DC
	1st Stage Emitter Bias (Signal)	R16	25	Figure 5.29	–0.34512V DC
	1st Stage Emitter Bias (Reference)	R20	26	Figure 5.29	–0.34531V DC
	1st Stage Emitter Bias	R17	27	Figure 5.29	–0.34565V DC
	+ Bootstrap Voltage	CR7 (Cathode)	28	Figure 5.29	+5.0446V DC
	– Bootstrap Voltage	CR8 (Anode)	29	Figure 5.29	–5.0639V DC
	Bootstrap Common	J5-1	30	Figure 5.29	+0.095790V DC
	Input Bias Network Divider Bias	R9	31	Figure 5.29	+0.42076V DC
	Input Bias Network Diode Drop	Q3 (Collector)	32	Figure 5.29	+0.21343V DC
	Current Sink Op Amp Output	R55	33	Figure 5.29	–0.99200V DC
	Isolator Output	TP1	34	Figure 5.29	+0.99998V DC
	Isolator X10 DR	J5-16	35	Figure 5.29	–0.54680V DC
	Isolator X1 DR	J5-15	36	Figure 5.29	–4.7223
Range: 1, Manual Connect Input Terminals to a –1.00000V DC	Isolator Op Amp – In	R15	23	Figure 5.29	+0.36620V DC
	Isolator Op Amp + In	R19	24	Figure 5.29	+0.36630V DC
	1st Stage Emitter Bias (Signal)	R16	25	Figure 5.29	–1.44490V DC
	1st Stage Emitter Bias (Reference)	R20	26	Figure 5.29	–1.44497V DC
	1st Stage Emitter Bias	R17	27	Figure 5.29	–1.44525V DC

Table 5.20 - Reference Isolator PCB, Isolator/Bootstrap Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	+ Bootstrap Voltage	CR7 (Cathode)	28	Figure 5.29	+3.9634V DC
	– Bootstrap Voltage	CR8 (Anode)	29	Figure 5.29	–6.1567V DC
	Bootstrap Common	J5-1	30	Figure 5.29	–1.00420V DC
	Input Bias Network Divider Bias	R9	31	Figure 5.29	–0.67852V DC
	Input Bias Network Diode Drop	Q3 (Collector)	32	Figure 5.29	–0.88592V DC
	Current Sink Op Amp Output	R55	33	Figure 5.29	+1.00380V DC
	Isolator Output	TP1	34	Figure 5.29	–0.99994V DC
	Isolator X10 DR	J5-16	35	Figure 5.29	–4.6812V DC
	Isolator X1 DR	J5-15	36	Figure 5.29	–0.54630V DC
Remove Input Voltage					



	Input Short	+.1V/.1 Rng	−1V/1 Rng
23	+1.34425	+1.44185	+0.36620
24	+1.34386	+1.44235	+0.36630
25	−0.44451	−0.34512	−1.44490
26	−0.44475	−0.34531	−1.44497
27	−0.44515	−0.34565	−1.44525
28	+4.9464	+5.0446	+3.9634
29	−5.1634	−5.0639	−6.1567
30	−0.004212	+.095790	−1.00420
31	+0.32148	+0.42076	−0.67852
32	+0.113454	+0.21343	−0.88592
33	−0.005905	−0.99200	+1.00380
34	−0.000002	+0.99998	−0.99994
35	−0.54680	−0.54680	−4.6812
36	−4.7223	−4.7223	−0.54630

Figure 5.29 - Isolator/Bootstrap Test Point Locations

Table 5.21 - Reference Isolator PCB, Ratio Reference Generator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV (S2) & RATIO (S5) Range: .1 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected to a DC voltage standard set to ±.100000. J103 (Ext Ref Hi) and J104 (Ext Ref Lo) connected to a DC voltage standard set to +10.0000.					NOTE: Shorting links from J101 to J103 & J102 to J104 must be disconnected before signal and reference voltages are applied NOTE: All measurements are referenced to TP4 (MECCA) NOTE: The ratio technique used in this DMM is 3-wire. Be careful to avoid ground loops and unreferenced power sources when using a minus signal (numerator) to prevent shock hazards to the operator and possible damage to associated test equipment
Display: .100000	Ref Op Amp + In	J7-E	37	Figure 5.30	+10.0000V DC
	Ref Op Amp – In	J7-D	38	Figure 5.30	+10.0016V DC
	Ref Op Amp Out	R57	4	Figure 5.30	+10.6459V DC
	+1V Ref Out	P5-18	11	Figure 5.30	+1.00009V DC
Set Ext Ref DC voltage standard to +5.0000. Display: .199999 or 0.20000.	Ref Op Amp + In	J7-E	37	Figure 5.30	+5.0000V DC
	Ref Op Amp – In	J7-D	38	Figure 5.30	+5.0017V DC
	Ref Op Amp Out	R57	4	Figure 5.30	+5.5578V DC
	+1V Ref Out	P5-18	11	Figure 5.30	+0.49933V DC
Set Ext Ref DC voltage standard to +2.0000. Display: 0.50000	Ref Op Amp + In	J7-E	37	Figure 5.30	+2.0000V DC
	Ref Op Amp – In	J7-D	38	Figure 5.30	+2.0017V DC
	Ref Op Amp Out	R57	4	Figure 5.30	+2.5432V DC
	+1V REf Out	P5-18	11	Figure 5.30	+0.19940V DC
Disable Ratio switch, S5, to return DMM to DCV Function and remove Ext Ref Input Cable.					

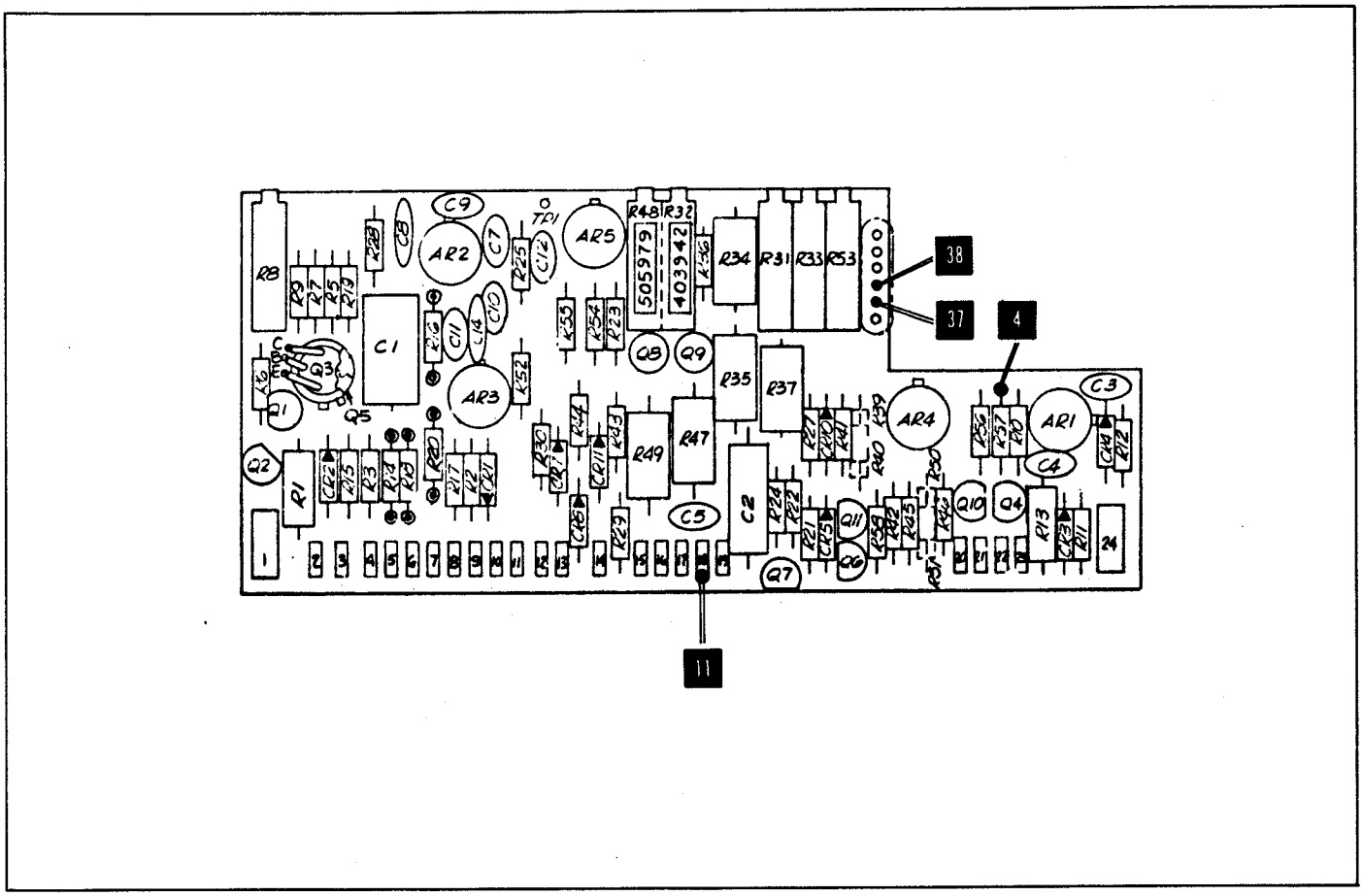


Figure 5.30 - Ratio Reference Generator Test Point Locations

Table 5.22 - Digitizer PCB, HV Buffer Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 100, Manual Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Assembly is to be mounted on Extender PCB, P/N 403993					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
	HV Buffer Op Amp – In	R14	1	Figure 5.31	+7.4196V DC
	HV Buffer Op Amp + In	R15	2	Figure 5.31	+7.4201V DC
	1st Stage Source Bias	R19	3	Figure 5.31	+2.0093V DC
	+300V Source	J3-4	4	Figure 5.31	+263.35V DC
	–300V Source	J3-5	5	Figure 5.31	–263.75V DC
	Plus Regulator Bias	R29	6	Figure 5.31	+134.50V DC
	Plus Zener Reference Voltage	CR10 (Cathode)	7	Figure 5.31	+9.8629V DC
	Plus Op Amp Drive Voltage	AR1-7	8	Figure 5.31	+9.3336V DC
	Op Amp Output	R27	9	Figure 5.31	–0.07155V DC
	Minus Reference Voltage	AR6-13	10	Figure 5.31	–9.1338V DC
	Minus Op Amp Drive Voltage	AR1-4	11	Figure 5.31	–8.5548V DC
	Minus Regulator Bias	R31	12	Figure 5.31	–135.00V DC
	Current Generator Emitter Bias	R35	13	Figure 5.31	–0.69025V DC
	HV Buffer Output	TP1	14	Figure 5.31	+0.00007V DC

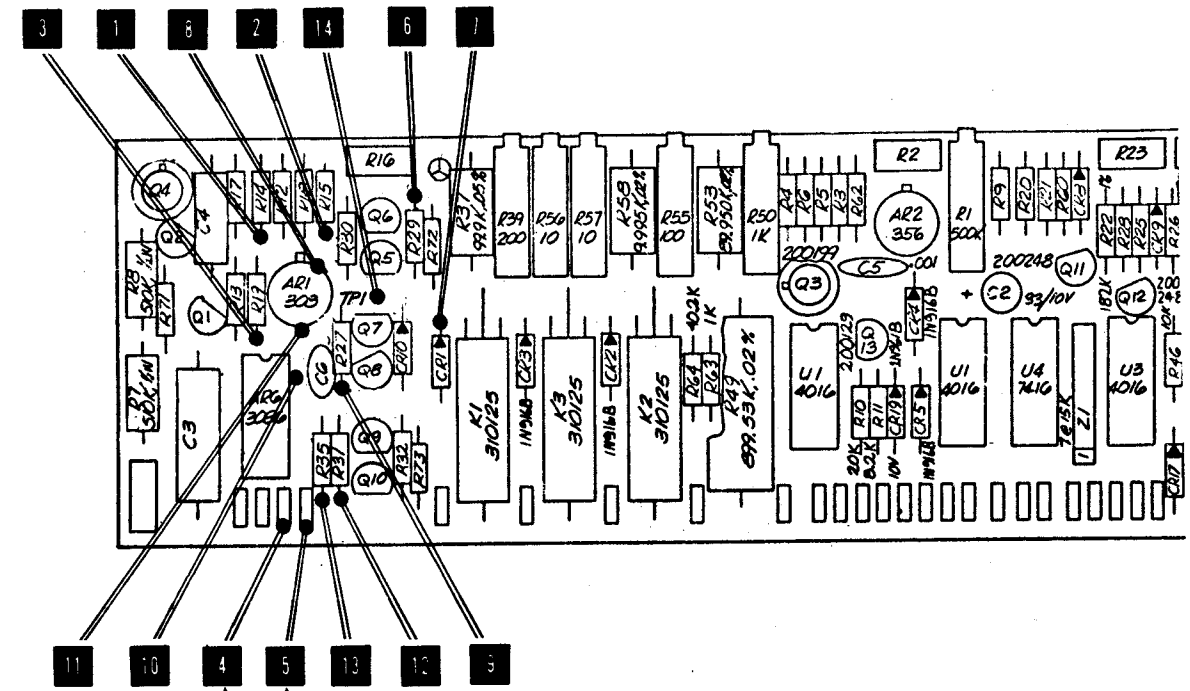


Figure 5.31 - HV Buffer Test Point Locations

Table 5.23 - Digitizer PCB, Switching/Integrator/Null Detector Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 1, Manual Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Assembly is to be mounted on Extender PCB, P/N 403993					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB NOTE: Ext Trig Scope at TP1, SID, Main PCB
	Buffer Op Amp – Input	R62	15	Figure 5.32	+10.1640V DC
	Buffer Op Amp + Input	R64	16	Figure 5.32	+10.1707V DC
	Buffer 1st Stage Source Bias	Q13 (Collector)	17	Figure 5.32	+1.39200V DC
	Buffer Current Generator Base Bias	CR19 (Anode)	18	Figure 5.32	–9.3282V DC
	Buffer Current Generator Emitter Bias	R10	19	Figure 5.32	–9.9560V DC
Remove input jumper. Connect input to DC standard set to +1.0000V DC	SID	J3-18	A	Figure 5.32	Waveform 1
	CPD	U4-8	B	Figure 5.32	Waveform 2
	$\overline{\text{Reset}}$	J3-21	C	Figure 5.32	Waveform 3
	AZ	J3-20	D	Figure 5.32	Waveform 4
	$\overline{\text{SIF}}$	J3-19	E	Figure 5.32	Waveform 5
	AZC	J3-23	F	Figure 5.32	Waveform 6
	– RD	J3-13	G	Figure 5.32	Waveform 7
	CID	U4-12	H	Figure 5.32	Waveform 8
	IND	U4-6	I	Figure 5.32	Waveform 9
	Reference Cap Switching, +	U3-3	J	Figure 5.32	Waveform 10
	Reference Cap Switching, –	U3-2	K	Figure 5.32	Waveform 11
	Measurement Cap Switching, +	U1-2	L	Figure 5.32	Waveform 12

Table 5.23 - Digitizer PCB, Switching/Integrator/Null Detector Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Measurement Cap Switching, –	U1-10	M	Figure 5.32	Waveform 13
	Buffer Input Switching	U2-4	N	Figure 5.32	Waveform 14
	Buffer Output Switching	TP2	O	Figure 5.32	Waveform 15
	Integrator Output	TP3	P	Figure 5.32	Waveform 16
	Minus Feed-Forward Switching	R25	Q	Figure 5.32	Waveform 17
	Plus Feed-Forward Switching	R26	R	Figure 5.32	Waveform 18
	Null Detector Input (1st Stage)	CR13 (Cathode)	S	Figure 5.32	Waveform 19
	Null Detector Input (2nd Stage)	R51	T	Figure 5.32	Waveform 20
	Null Detector Output	J3-29	U	Figure 5.32	Waveform 21
Change input to –1.9900V DC	AZ	J3-20	D	Figure 5.32	Waveform 22
	AZC	J3-23	F	Figure 5.32	Waveform 23
	+ RD	J3-12	V	Figure 5.32	Waveform 24
	IND	U4-6	I	Figure 5.32	Waveform 25
	Reference Cap Switching, +	U3-3	J	Figure 5.32	Waveform 26
	Reference Cap Switching, –	U3-2	K	Figure 5.32	Waveform 27
	Measurement Cap Switching, +	U1-2	L	Figure 5.32	Waveform 28
	Measurement Cap Switching, –	U1-10	M	Figure 5.32	Waveform 29
	Buffer Input Switching	U2-4	N	Figure 5.32	Waveform 30

Table 5.23 - Digitizer PCB, Switching/Integrator/Null Detector Subassembly Performance Test continued

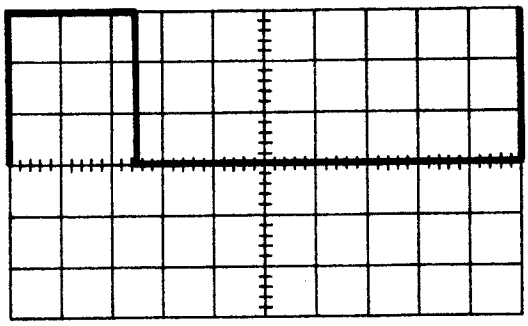
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Buffer Output Switching	TP2	O	Figure 5.32	Waveform 31
	Integrator Output	TP3	P	Figure 5.32	Waveform 32
	Minus Feed-Forward Switching	R25	Q	Figure 5.32	Waveform 33
	Plus Feed-Forward Switching	R26	R	Figure 5.32	Waveform 34
	Null Detector Input (1st Stage)	CR13 (Cathode)	S	Figure 5.32	Waveform 35
	Null Detector Input (2nd Stage)	R51	T	Figure 5.32	Waveform 36
	Null Detector Output	J3-29	U	Figure 5.32	Waveform 37
Remove input cables and extender PCB					

WAVEFORMS FOR TABLE 5.23

1 (NO.)

SID

J3-18



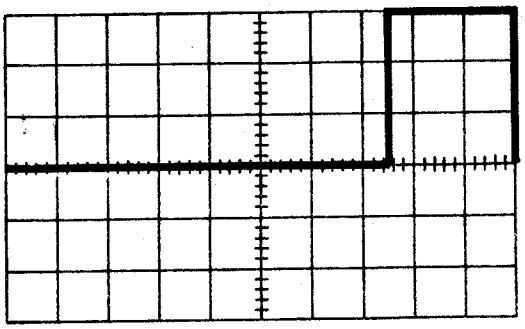
5.0 (V/DIV)

20 mS (S/DIV)

2 (NO.)

CPD

U4-8



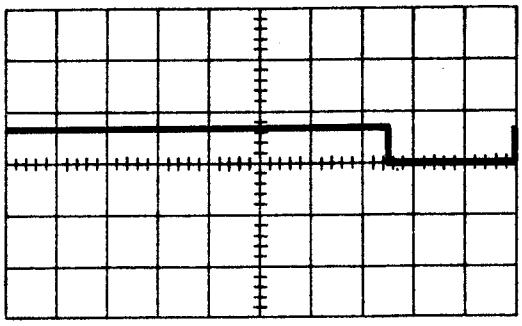
5.0 (V/DIV)

20 mS (S/DIV)

3 (NO.)

$\overline{\text{RESET}}$

J3-21



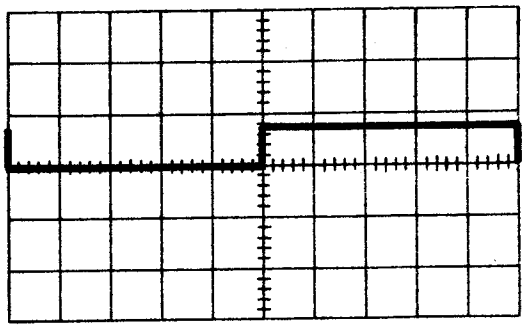
5.0 (V/DIV)

20 mS (S/DIV)

4 (NO.)

AZ

J3-20



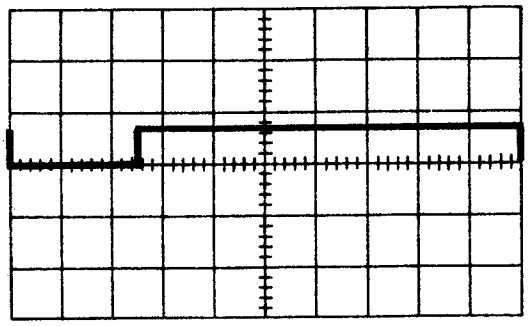
5.0 (V/DIV)

20 mS (S/DIV)

5 (NO.)

$\overline{\text{SIF}}$

J3-19



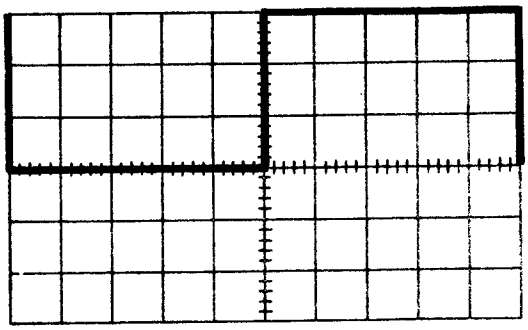
5.0 (V/DIV)

20 mS (S/DIV)

6 (NO.)

AZC

J3-23



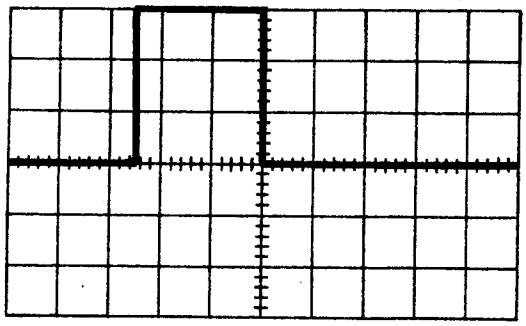
5.0 (V/DIV)

20 mS (S/DIV)

WAVEFORMS FOR TABLE 5.23 continued

7 (NO.) –RD

J3-13

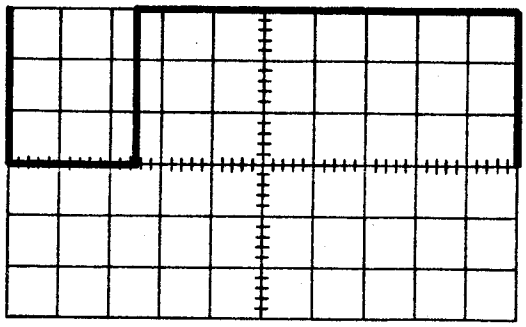


5.0 (V/DIV)

20 mS (S/DIV)

8 (NO.) CID

J4-12

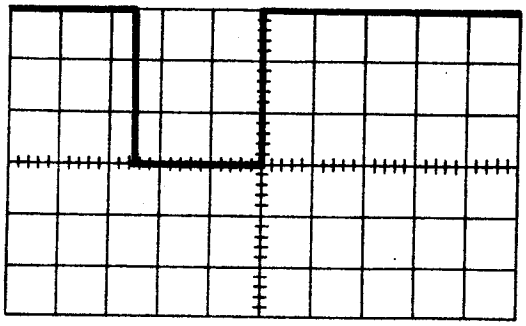


5.0 (V/DIV)

20 mS (S/DIV)

9 (NO.) IND

U4-6

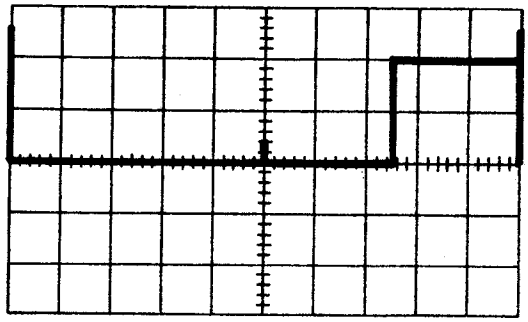


5.0 (V/DIV)

20 mS (S/DIV)

10 (NO.) REF CAP SWITCHING, +

U3-3

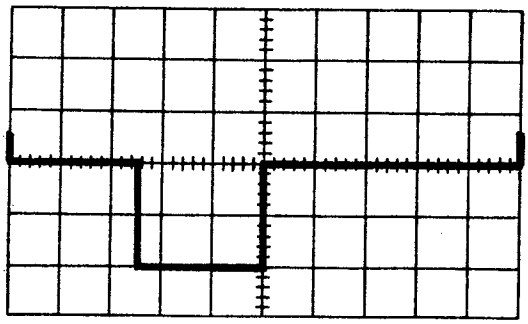


0.5 (V/DIV)

20 mS (S/DIV)

11 (NO.) REFERENCE CAP, –

U3-2

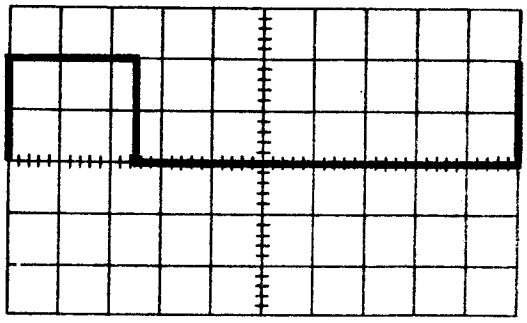


0.5 (V/DIV)

20 mS (S/DIV)

12 (NO.) MEASUREMENT CAP SWITCHING, +

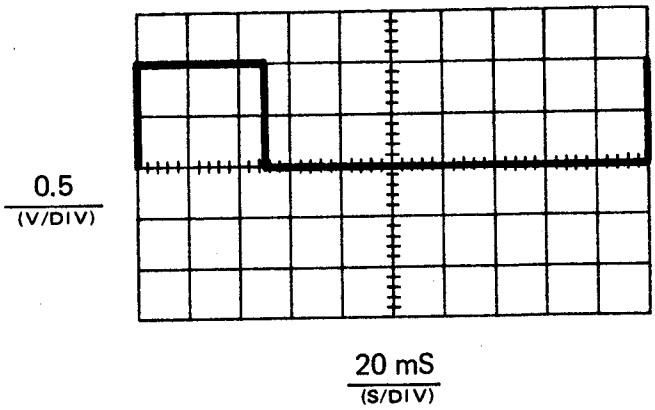
U1-2



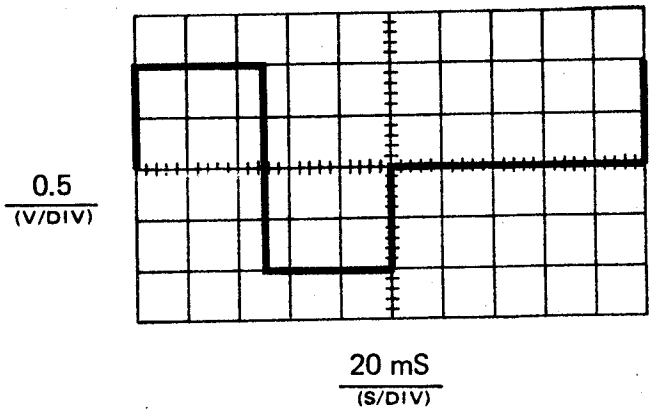
0.5 (V/DIV)

20 mS (S/DIV)

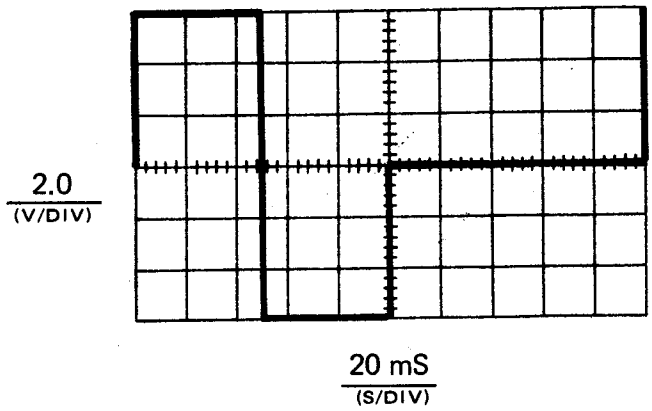
13 (NO.) MEASUREMENT CAP SWITCHING, – U1-10



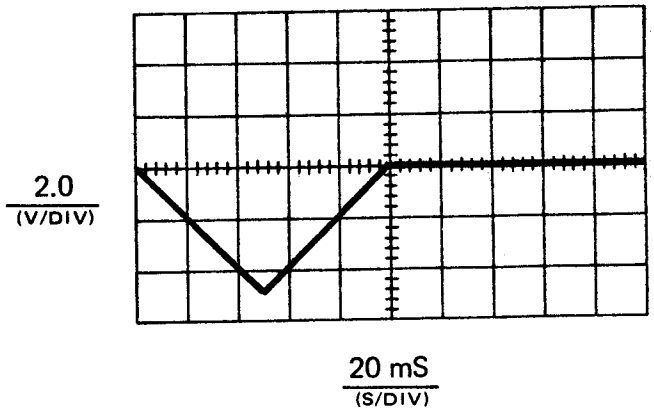
14 (NO.) BUFFER INPUT SWITCHING U2-4



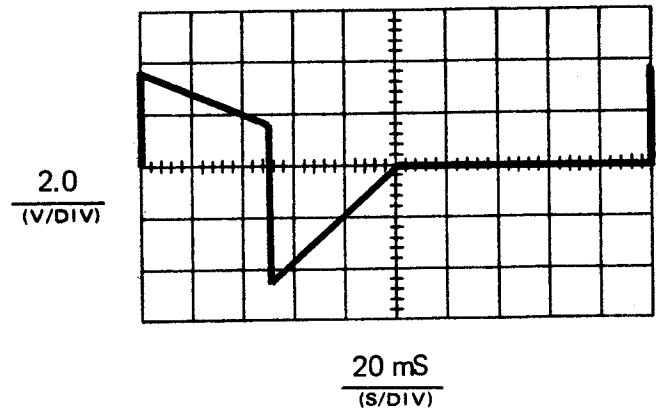
15 (NO.) BUFFER OUTPUT SWITCHING TP2



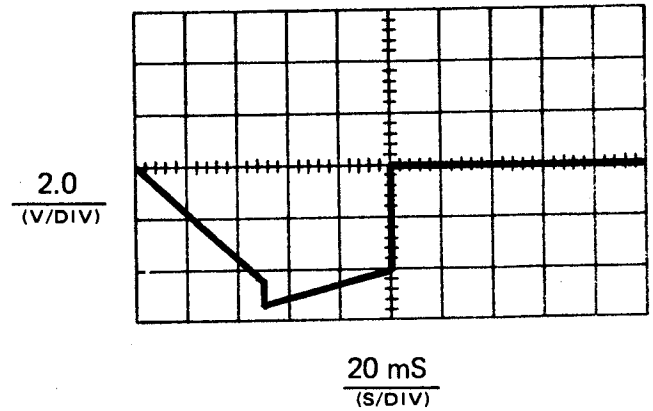
16 (NO.) INTEGRATOR OUTPUT TP3



17 (NO.) MINUS FEED FORWARD SWITCHING R25

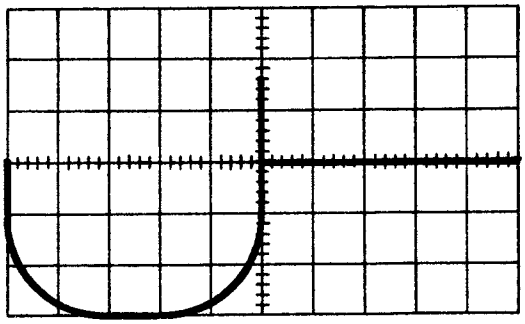


18 (NO.) PLUS FEED FORWARD SWITCHING R26



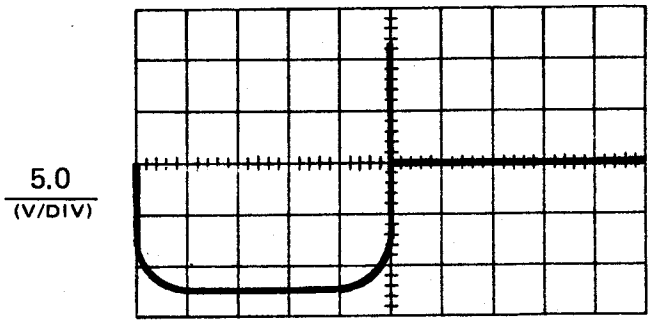
19 (NO.) NULL DETECTOR INPUT (1st STAGE)

CR13 (CATHODE)



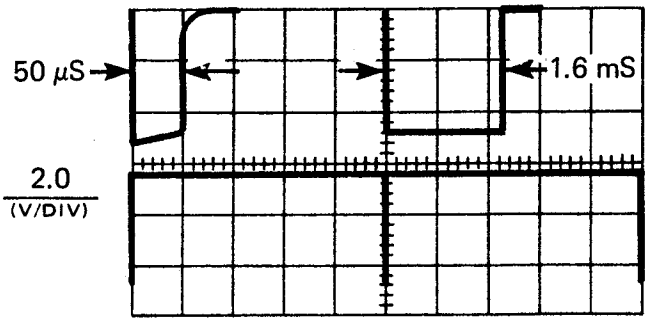
20 (NO.) NULL DETECTOR INPUT (2nd STAGE)

R51



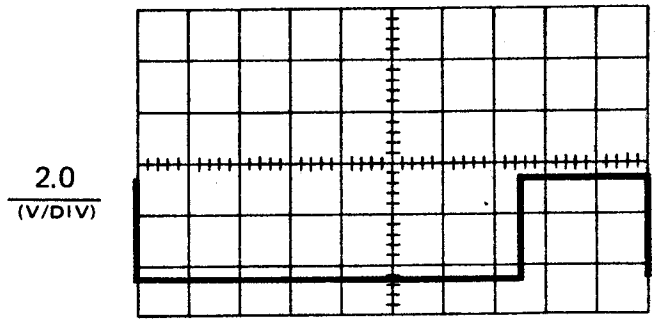
21 (NO.) NULL DETECTOR OUTPUT (−1.90000)

J3-29



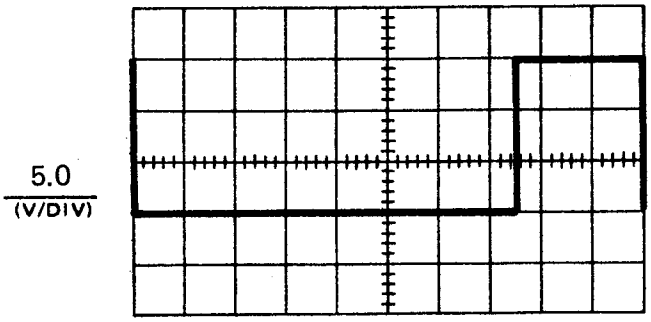
22 (NO.) AZ

J3-20



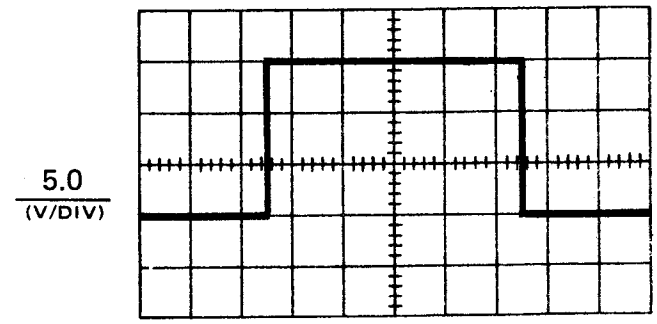
23 (NO.) AZC

J3-23



24 (NO.) + RD

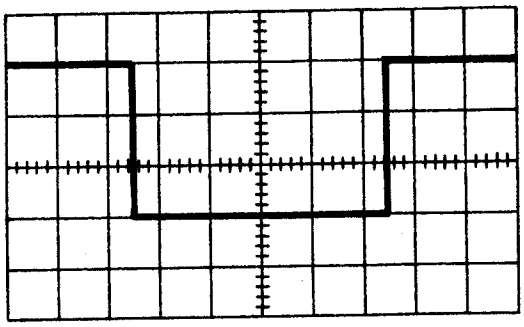
J3-12



WAVEFORMS FOR TABLE 5.23 continued

25 (NO.) IND

U4-6

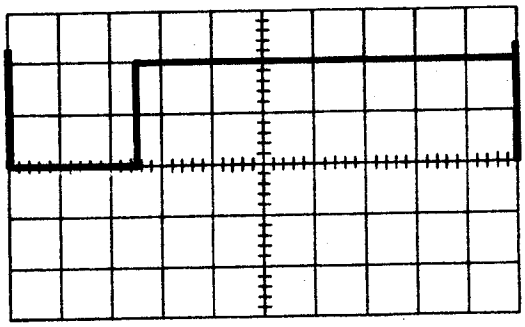


5.0 (V/DIV)

20 mS (S/DIV)

26 (NO.) REFERENCE CAP SWITCHING, +

U3-3

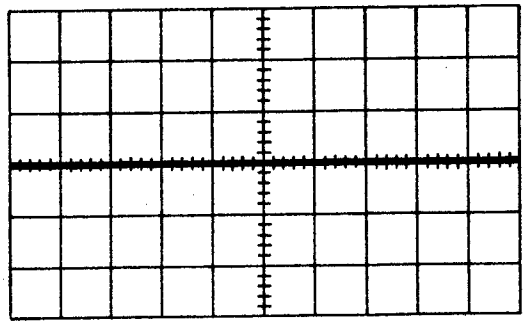


0.5 (V/DIV)

20 mS (S/DIV)

27 (NO.) REFERENCE SWITCHING CAP, –

U3-2

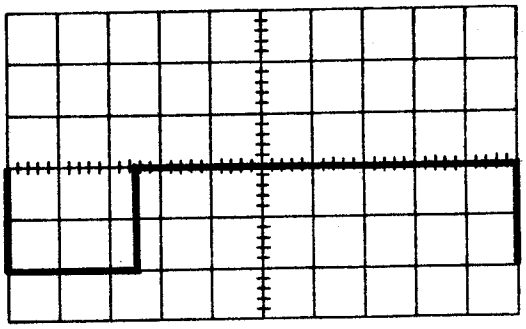


0.5 (V/DIV)

20 mS (S/DIV)

28 (NO.) MEASUREMENT CAP SWITCHING, +

U1-2

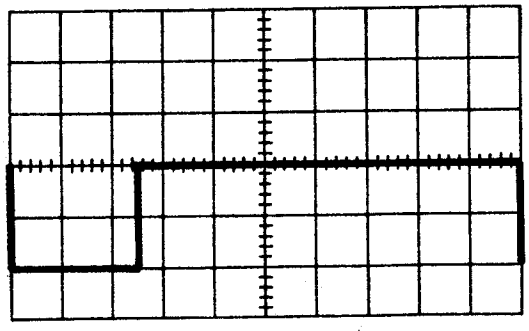


1.0 (V/DIV)

20 mS (S/DIV)

29 (NO.) MEASUREMENT SWITCHING CAP, –

U1-10

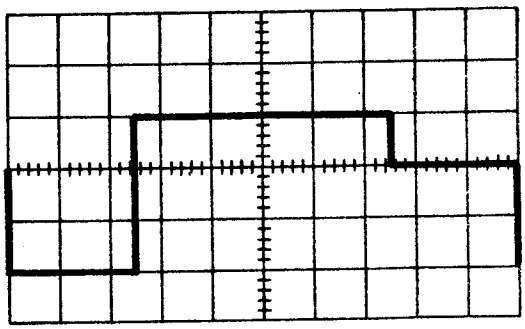


1.0 (V/DIV)

20 mS (S/DIV)

30 (NO.) BUFFER INPUT SWITCHING

U2-4

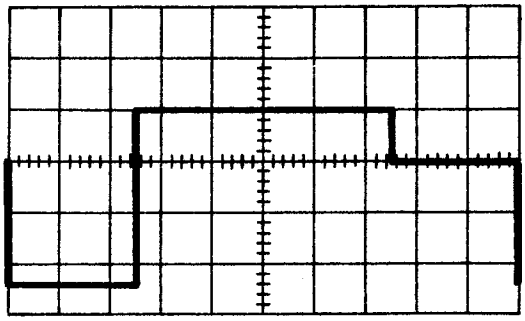


1.0 (V/DIV)

20 mS (S/DIV)

31 (NO.) BUFFER OUTPUT SWITCHING

TP2

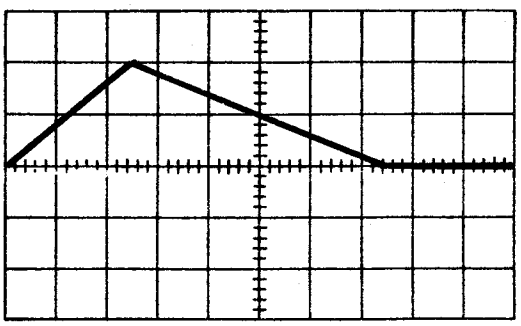


5.0 (V/DIV)

20 mS (S/DIV)

32 (NO.) INTEGRATOR OUTPUT

TP3

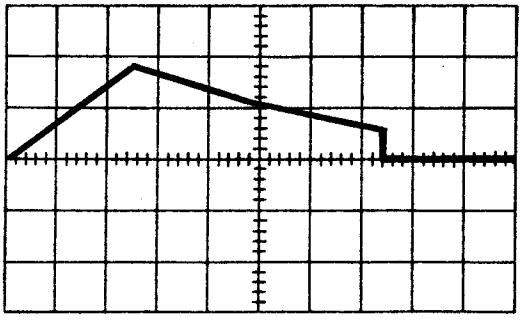


5.0 (V/DIV)

20 mS (S/DIV)

33 (NO.) MINUS FEED FORWARD SWITCHING

R25

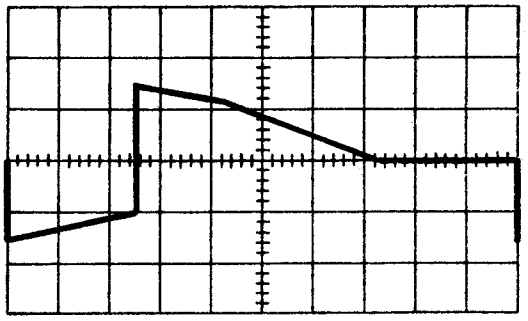


5.0 (V/DIV)

20 mS (S/DIV)

34 (NO.) PLUS FEED FORWARD SWITCHING

R26

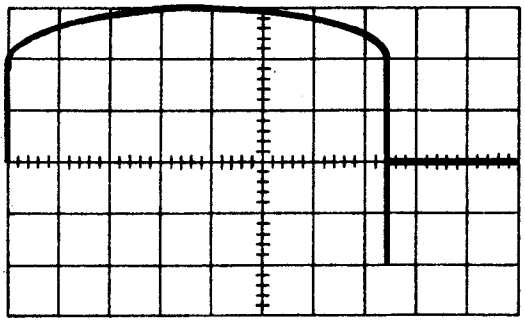


(V/DIV)

20 mS (S/DIV)

35 (NO.) NULL DETECTOR INPUT (1st STAGE)

CR13 (CATHODE)

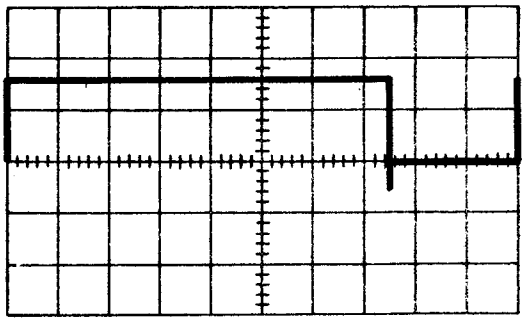


0.2 (V/DIV)

20 mS (S/DIV)

36 (NO.) NULL DETECTOR INPUT (2nd STAGE)

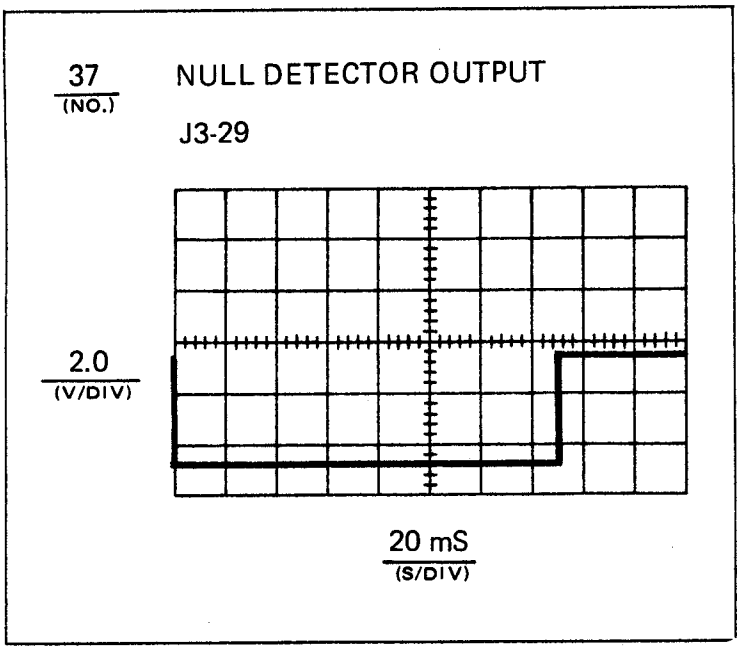
R51



10.0 (V/DIV)

20 mS (S/DIV)

WAVEFORMS FOR TABLE 5.23 continued



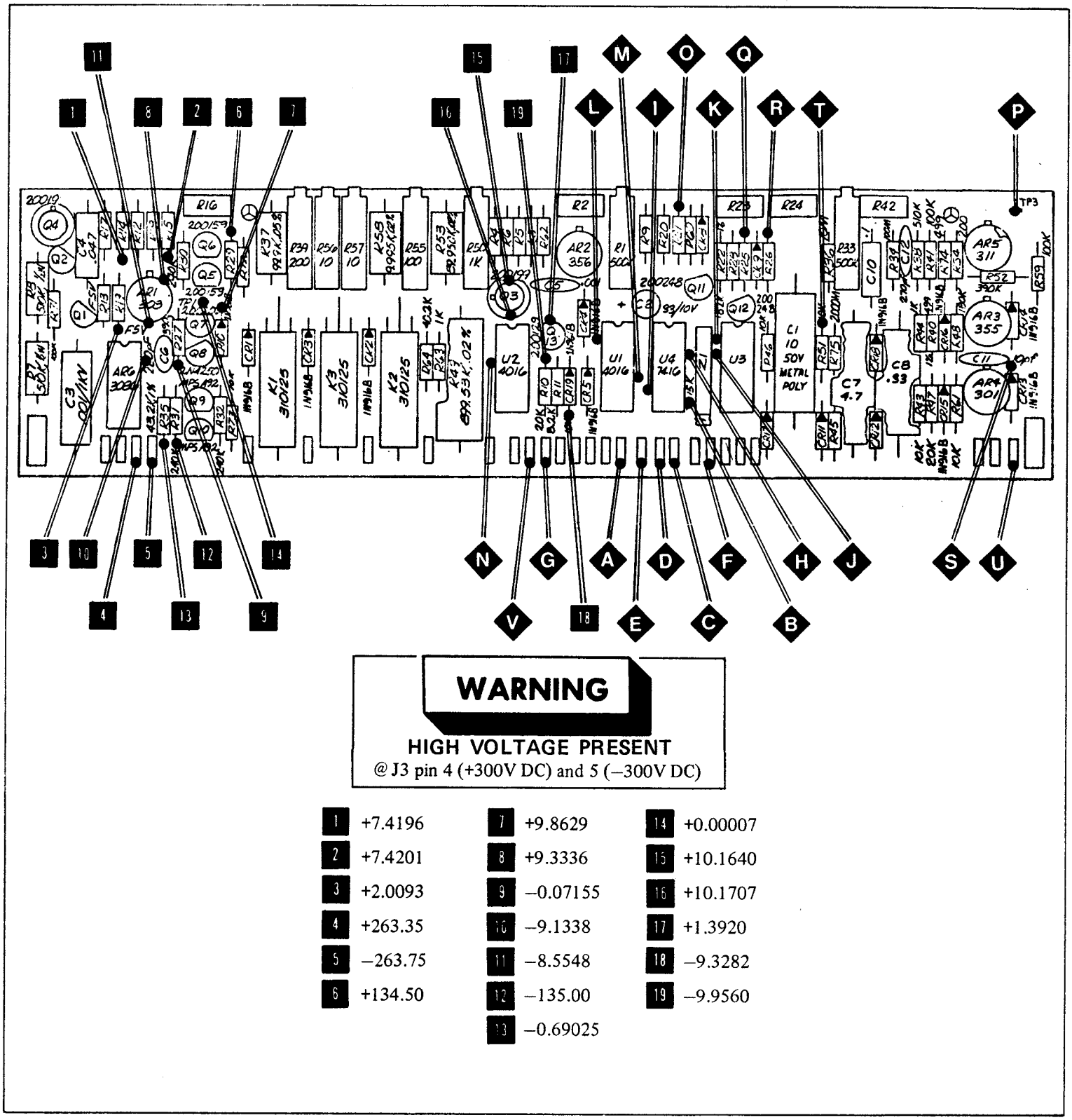


Figure 5.32 - Switching/Integrator/Null Detector Test Point Locations

Table 5.24 - AC (Averaging) Converter PCB, Subassembly Performance Test

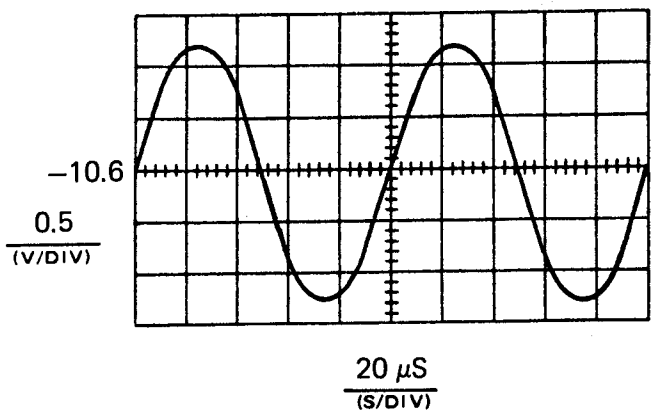
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV Range: 1, Manual Filter: IN (automatically selected) Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Shield must be removed and assembly placed on extender PCB, 403993 for test					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
	Scaling Op Amp – Input	R3	1	Figure 5.33	+1.42425V DC
	Scaling Op Amp + Input	R4	2	Figure 5.33	+1.42408V DC
	1st Stage Source Load Bias	R15	3	Figure 5.33	–14.506V DC
	Scaling Op Amp Output	AR1-6	4	Figure 5.33	–10.677V DC
	Rectifier Output Driver Bias	CR6 (Anode)	5	Figure 5.33	+13.260V DC
	Rectifier Output Driver Bias	CR7 (Cathode)	6	Figure 5.33	–12.910V DC
	PNP Output Driver Emitter Bias	R7	7	Figure 5.33	+13.896V DC
	NPN Output Driver Emitter Bias	R8	8	Figure 5.33	–13.500V DC
	Rectifier Output	CR8 (Cathode)	9	Figure 5.33	0V (.3V p-p Switching Noise)
Remove jumper. Connect input to a signal (function) generator set to 1.9V RMS @ 10 kHz	Scaling Op Amp Output	AR1-6	A	Figure 5.33	Waveform 1
	Scaling Rectifier Output	CR8 (Cathode)	B	Figure 5.33	Waveform 2
	Minus Rectified Output	CR8 (Anode)	C	Figure 5.33	Waveform 3
	Plus Rectified Output	CR9 (Cathode)	D	Figure 5.33	Waveform 4
	Plus Output	J4-11	E	Figure 5.33	Waveform 5 (Note ripple)
	Minus Output	J4-10	F	Figure 5.33	Waveform 6 (Note ripple)
Remove voltage, cables, extender PCB, and replace shields					

INPUT
1.9V RMS @ 10 kHz/ 1 RNG

WAVEFORMS FOR TABLE 5.24

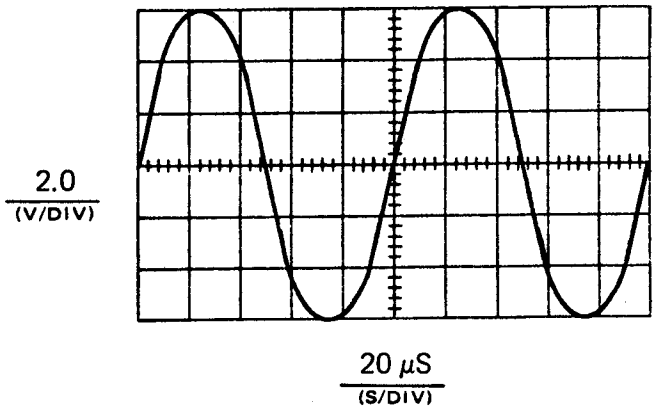
REF: TP4 (MECCA) MAIN PCB
COUPLING: DC, UNLESS NOTED

1 (NO.) SCALING OP AMP OUTPUT
AR1-6

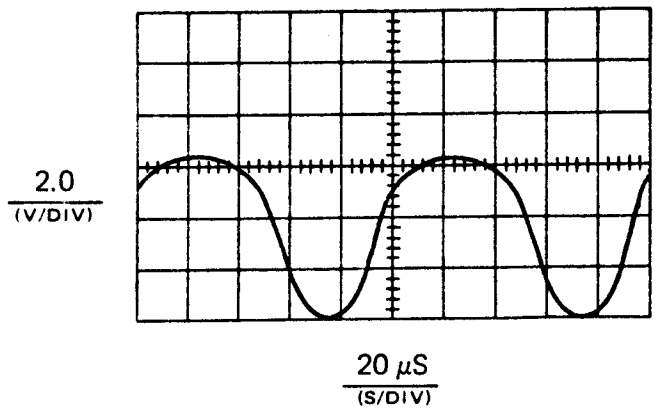


AC COUPLED

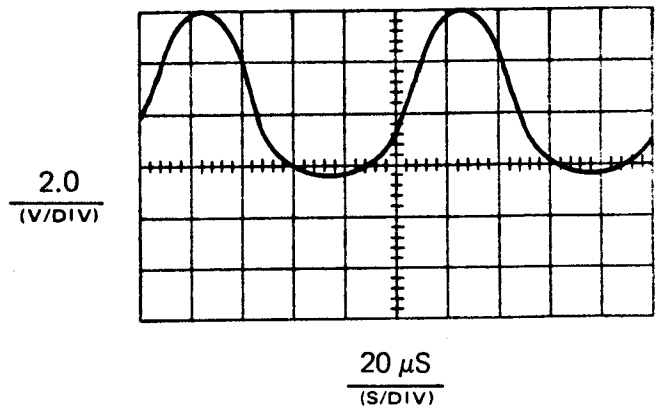
2 (NO.) SCALING RECTIFIER OUTPUT
CR8 (CATHODE)



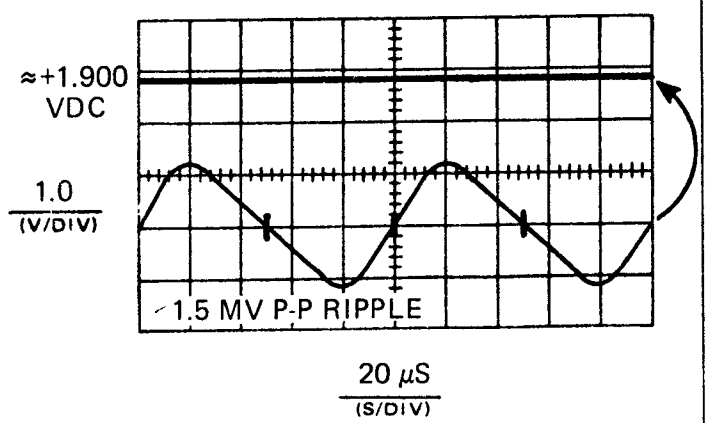
3 (NO.) MINUS RECTIFIED OUTPUT
CR8 (ANODE)



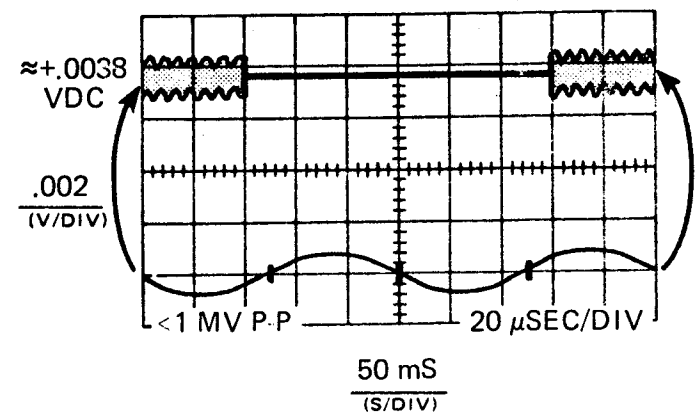
4 (NO.) PLUS RECTIFIED OUTPUT
CR9 (CATHODE)



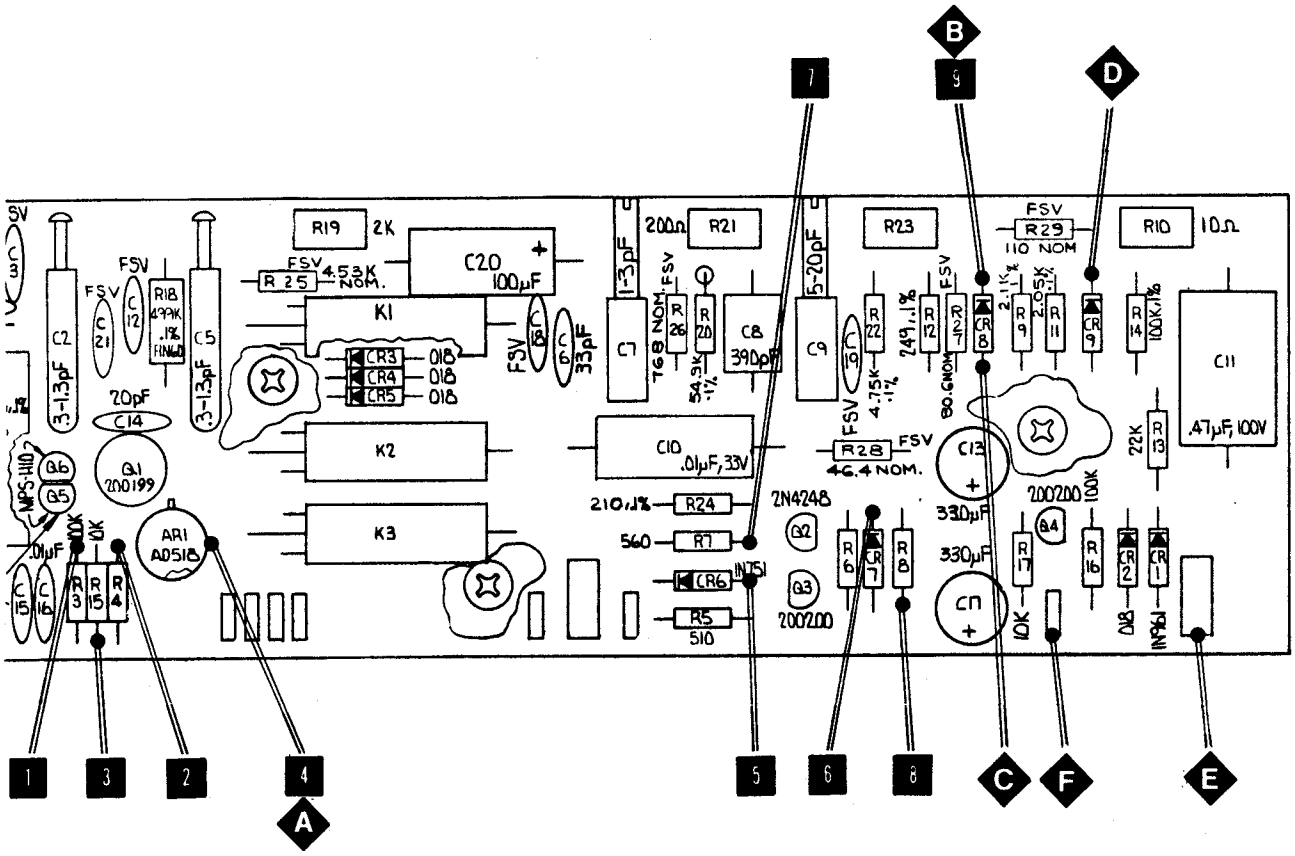
5 (NO.) PLUS OUTPUT
J4-11



6 (NO.) MINUS OUTPUT
J4-10



EXT TRIG; TP1 (SID) MAIN PCB

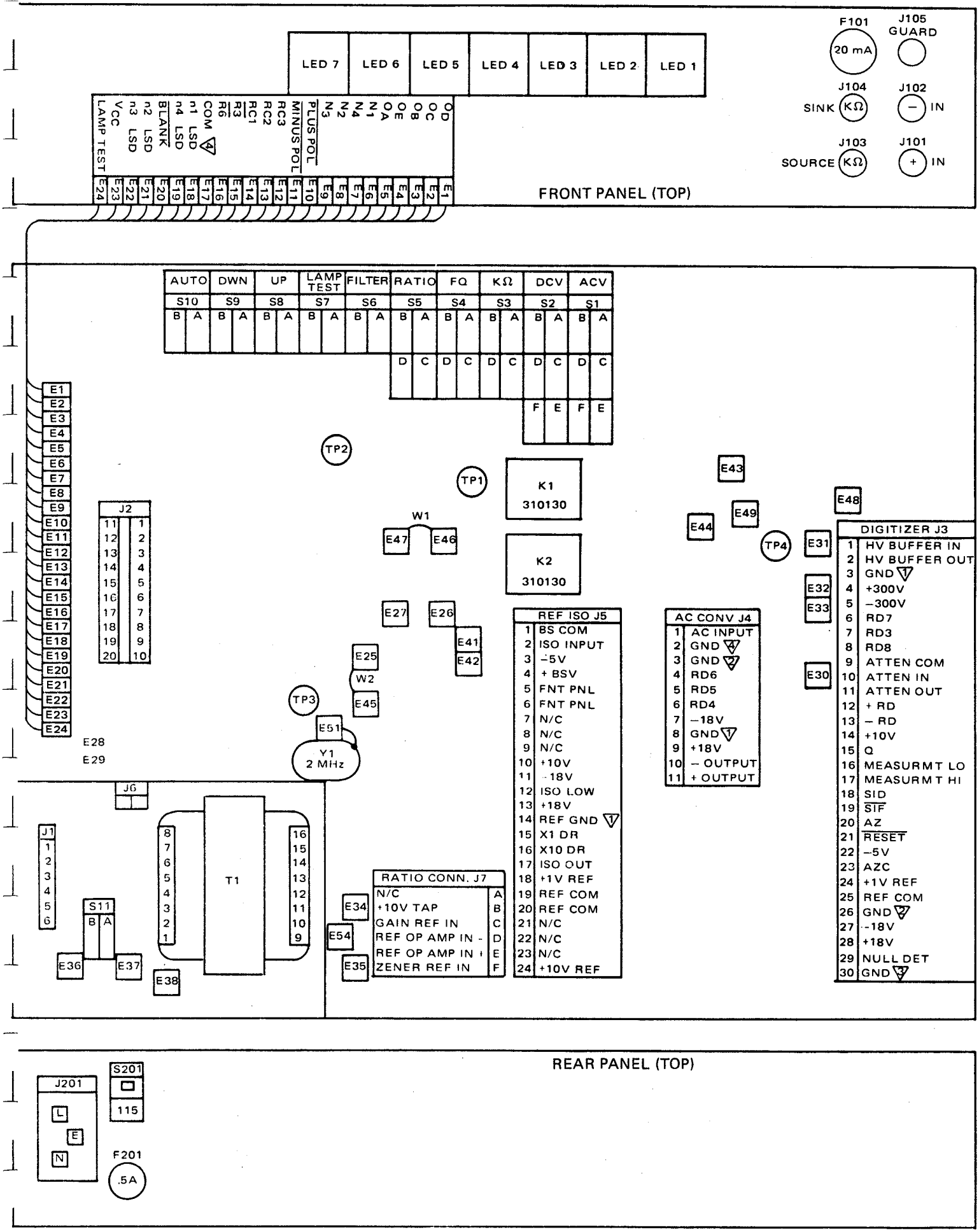


1 +1.42425
2 +1.42408
3 −14.506
4 −10.677
5 +13.260
6 −12.910
7 +13.896
8 −13.500
9 0V (.3 mV P-P Switching Noise)

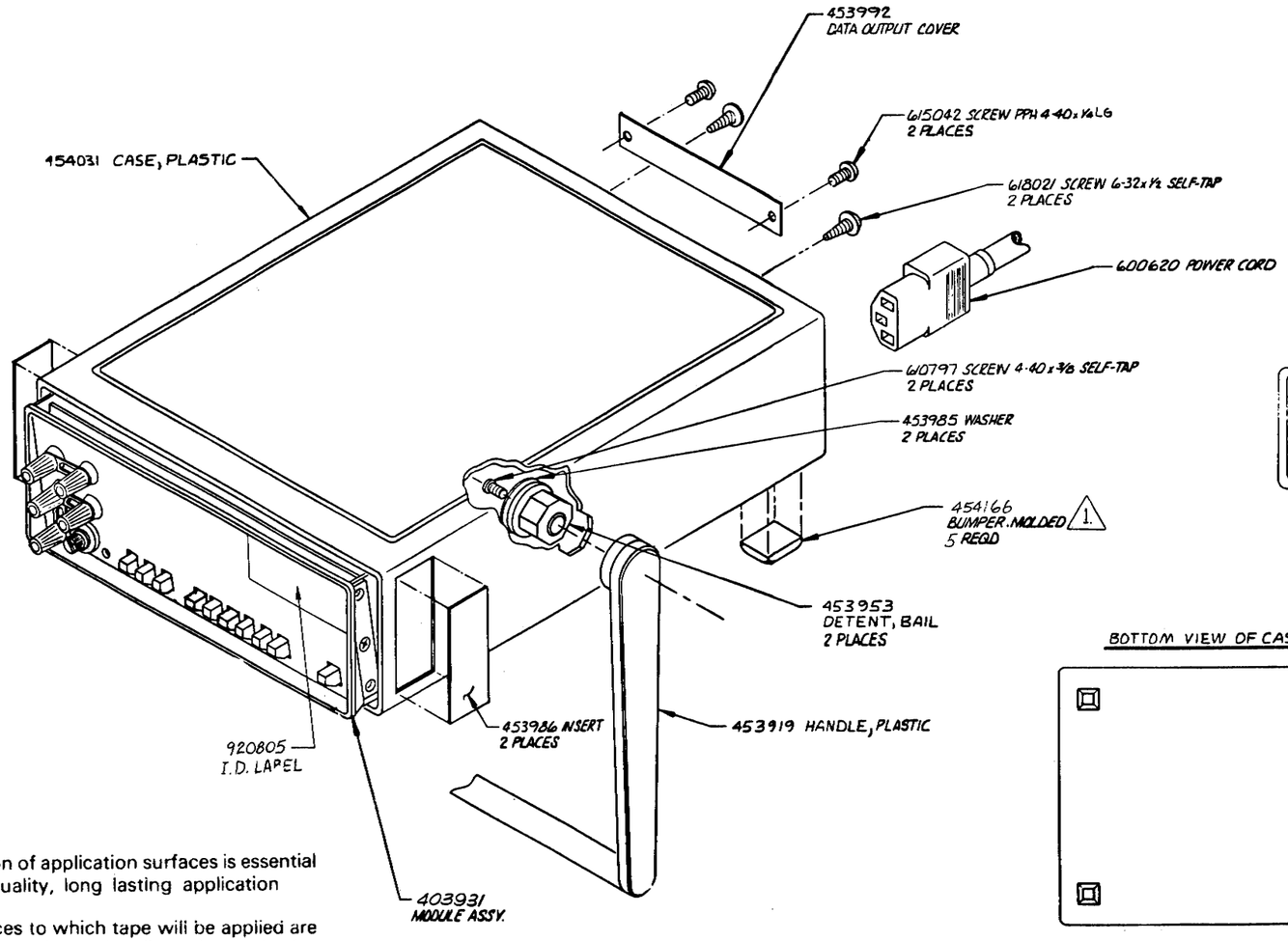
Figure 5.33 - Averaging AC Converter Test Point Locations

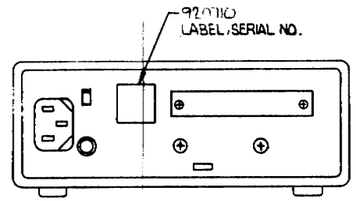
Table 5.25 - 5100AF Interconnect Pinouts

J101	–	"+" IN (DCV, ACV, KΩ)/S1-D-2
J102	–	"–" IN (DCV, ACV, KΩ)/S4-D-2
J103	–	KΩ Source/Ext Ref "+"/F101
J104	–	KΩ Sink/Ext Ref "–"/S3-A-3, S5-B-3
J105	–	GUARD/E52
F101	–	Fused (Ratio) Ext Ref Input J103 to S5-A-2
S1	–	ACV
S2	–	DCV
S3	–	KΩ
S4	–	FQ (Inoperative)
S5	–	Ratio X10
S6	–	Filter
S7	–	Lite Test
S8	–	Up
S9	–	Down
S10	–	Auto
S11	–	Power
E1	–	0_D
E2	–	0_C
E3	–	0_B
E4	–	0_E
E5	–	0_A
E6	–	N_1
E7	–	N_4
E8	–	N_2
E9	–	N_3
E10	–	$\overline{\text{Plus Pol}}$
E11	–	$\overline{\text{Minus Pol}}$
E12	–	RC3
E13	–	RC2
E14	–	RC1
E15	–	$\overline{R3}$
E16	–	$\overline{R6}$
E17	–	Dig Com
E18	–	LSD n1
E19	–	LSD n4
E20	–	$\overline{\text{Blank}}$
E21	–	LSD N_2
E22	–	LSD N_3
E23	–	V_{CC} (MECCA)
E24	–	Lamp Test
E25	–	W2-Filter Output
E26	–	E42-Iso Input/R29, S1-C-3, S6-A-3
E27	–	S1-B-2/R28
E28	–	(Not Used)
E29	–	(Not Used)
E30	–	Attenuator In
E31	–	HV Buffer In
E32	–	+300V
E33	–	–300V
E34	–	+300V
E35	–	–300V
E36	–	F201 to S11-B-3 (Line ACV)
E37	–	J201-N to S11-A-3 (Neutral)
E38	–	Earth Gnd to E53
E39	–	S4-B-3
E40	–	+18V, E50
E41	–	Shield to BSC
E42	–	Isolator Input/E26
E43	–	S2-B-1, S2-E-1, K1-8, S3-B-2, & R22
E44	–	R27, K1-9, S2-A-1, & S2-B-3
E45	–	W2-Filter Output
E46	–	W1/R29
E47	–	R28/W1
E48	–	R22, R26
E49	–	R26, R27
E50	–	+18V, E40
E51	–	Gnd ▽4 to Crystal Can
E52	–	Chassis, xfmr core, & Guard (J105)
E53	–	Earth Gnd to frnt pnl overlay
E54	–	Mecca (shield for E34/35)
J1	–	Voltage select PCB Assy. – 403928
J2	–	Data Output (Not Used)
J3	–	Digitizer PCB Assy. – 403935
J4	–	AC (Avg) Converter PCB Assy. – 403905
J5	–	Ref Isolator PCB Assy. – 403934
J6	–	Data Output Isolated PWR (Not Used)
J7	–	On Ref Iso PCB, Ratio Input Conn.
J201	–	Line Power Conn.
F201	–	Line Fuse
S201	–	Line Select SW.


LED 7
LED 6
LED 5
LED 4
LED 3
LED 2
LED 1
F101
20 mA
J105
GUARD
J104
SINK KΩ
J102
IN
J103
SOURCE KΩ
J101
IN
LAMP TEST
Vcc
n3 LSD
n2 LSD
BLANK
n4 LSD
n1 LSD
COM
R6
R3
RC1
RC2
RC3
MINUS POL
PLUS POL
N3
N2
N4
N1
OA
OE
OB
OC
OD
FRONT PANEL (TOP)
AUTO
DWN
UP
LAMP TEST
FILTER
RATIO
FQ
KΩ
DCV
ACV
TP2
TP1
K1
310130
K2
310130
W1
W2
J2
E43
E44
E49
E48
TP4
E31
E32
E33
E30
DIGITIZER J3
1 HV BUFFER IN
2 HV BUFFER OUT
3 GND
4 +300V
5 −300V
6 RD7
7 RD3
8 RD8
9 ATTEN COM
10 ATTEN IN
11 ATTEN OUT
12 + RD
13 − RD
14 +10V
15 Q
16 MEASURMT LO
17 MEASURMT HI
18 SID
19 SIF
20 AZ
21 RESET
22 −5V
23 AZC
24 +1V REF
25 REF COM
26 GND
27 -18V
28 +18V
29 NULL DET
30 GND
REF ISO J5
1 BS COM
2 ISO INPUT
3 −5V
4 + BSV
5 FNT PNL
6 FNT PNL
7 N/C
8 N/C
9 N/C
10 +10V
11 -18V
12 ISO LOW
13 +18V
14 REF GND
15 X1 DR
16 X10 DR
17 ISO OUT
18 +1V REF
19 REF COM
20 REF COM
21 N/C
22 N/C
23 N/C
24 +10V REF
AC CONV J4
1 AC INPUT
2 GND
3 GND
4 RD6
5 RD5
6 RD4
7 −18V
8 GND
9 +18V
10 − OUTPUT
11 + OUTPUT
RATIO CONN. J7
N/C A
+10V TAP B
GAIN REF IN C
REF OP AMP IN - D
REF OP AMP IN + E
ZENER REF IN F
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20 E21 E22 E23 E24
E28
E29
E27
E26
E41
E42
E25
E45
TP3
E51
Y1
2 MHz
J6
J1
T1
S11
E36
E37
E38
E34
E54
E35
REAR PANEL (TOP)
J201
L
E
N
S201
115
F201
.5A

SECTION 6 DRAWINGS





BOTTOM VIEW OF CASE

1. Proper preparation of application surfaces is essential to assure high quality, long lasting application

Assume all surfaces to which tape will be applied are contaminated — metals may be oily or dusty; plastics may be coated with mold release agents, dirt, etc.

Any surface contaminate will adversely affect adhesion and **must** be removed prior to application by solvent wiping.

a) Wet the application surface with a mild solvent such as isopropyl alcohol (rubbing alcohol) or heptane and wipe thoroughly.

b) Dry the surface with a lint free cloth before the solvent evaporates from the surface.

Bond strength can be improved with **firm** application pressure so as to develop intimate contact of adhesive to the bonding surface.

NOTES: UNLESS OTHERWISE SPECIFIED

DIGITAL MULTIMETER
MODEL 5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	400983	E

SCALE NONE | SHEET 1 OF 2

SHORTING BARS
P/N 600239
3 REQ'D.

VIEW M

453951 FRONT PANEL
4-40 PPH SCREW ¼" NOM. 2 PLCS
617052 #6 LOCK WASH. 2 PLCS
4 454020 FRT PNL OVERLAY
454127 SHIELD
SEE VIEW J, VIEW L & VIEW M, WIRE LIST.

600908 POST, BLACK
3 PLACES
617103 #6 FLAT WASH.
2 PLACES

920818 (F101)
FUSEHOLDER
920800
FUSE, 10MA

600907 POST, WHITE
617103 #6 FLT. WASH.
2 PLACES
(TOP TWO POSTS)

NOTE: ON J101, J102, J103 & J104 REPLACE ONE NUT WITH ONE WASH, #6 FLT. REF J105 RETAINS BOTH NUTS SEE VIEW J.

454012
PUSH BUTTON, WHITE
9 REQD
1 920504 CEMENT.

453989 RETAINER
2 PLACES

454127 SHIELD
(REF)

453946
PUSH BUTTON, GREEN
1 920504 CEMENT

SEE VIEW J

454215 (STOP)

403855
DISPLAY

TOP COVER REMOVED FOR CLARITY

403933
LOGIC & INTERCONNECTION

454235
CHASSIS

7301694 MYLAR
920786 ADHESIVE
SEE VIEW P

403935
DIGITIZER

403905
AC AVERAGING CONVERTER

403934
REFERENCE ISOLATOR

454236 - BRACKET
SCREW 4-40,
3/16 LG NOM - 2 REQD

453894
BUMPER STRIP

454240
COVER, TOP (SEE SHT 2)
615042 SCREW
PPH 4-40 x 1/4 LG

SCREW 4-40, 3/16 LG NOM
4 REQD
SEE VIEW E

920779 (F201)
FUSEHOLDER
920802
FUSE, .25AMP
SEE WIRE LIST

SCREW-PPH, 4-40 x 1/4" LG (NOM.)
HEX NUT, 4-40
SOLDER LUG
100046 CAP-1000V .01 SOLDER
FROM LUG TO FILTER CASE
MAKE LEADS AS SHORT AS POSSIBLE

310137
LINE FILTER
4-40 PAN HD SCREW, 1/2" LG NOM
4 FLAT WASHER - 2 REQD
#4 NUT, #4 LOCK WASHER
610820 SHOULDER WSHR, #4, 2 REQD
SEE WIRE LIST
2 PLCS

610596
NUT, EXPANSION
(2 PLACES)

SCREW PPH 4-40 x 1/4" NOM 2 REQD

454241
COVER, BOTTOM
4-40 SCREW, 3/16 LG NOM
454049
MYLAR INSERT
920789
CEMENT, SPRAY
920729 LABEL
SEE VIEW 'C'

454127 SHIELD (REF)

SEE DETAIL H & WIRE LIST

SEE VIEW J DETAIL K & WIRE LIST

VIEW L FRONT PANEL WIRING
(SEE WIRE LIST)

DETAIL A

610844 LOCK WASH.

610611 GROMMET
2 PLACES

CHASSIS (REF)

4-40 SCREW PFH 100° x 3/8" 3

610625 BeO WASHER 2

REGULATOR (REF)

610833 SHOULDER WASHER
#4 FLAT WASHER
#4 LOCK WASHER
#4 NUT 3

SEE VIEW B & WIRE LIST

403928 VOLTAGE SELECT
SCREW PFH 100°, 4-40 x 3/8 NOM

SCREW PFH 100°, 4-40 x 3/16 NOM
2 PLACES

454043 ROD,
POWER SWITCH

500034 FLAT CABLE

610777 TIE
6 PLACES

230338 (7818)
SEE DETAIL A & VIEW F

230337 (7918)
SEE DETAIL A & VIEW F

BROWN WIRE

BLUE WIRE
(AR4 PIN 2)

BROWN WIRE
(AR3 PIN 1)

BLUE WIRE

VIEW B

BROWN WIRE REF

.23 TYP

TRIM ALL LEADS ON AR3 & AR4 AS SHOWN

.40 TYP

AR3

AR4

.12 NOM TYP

10.75 NOM

11.63 NOM

500143
SHRINK TUBING

500034 FLAT CABLE REF

BLUE WIRE REF

DETAIL D

AR3 AR4
1 3 2 1 3 2

1 (IN)
3 (COM)
2 (OUT)
AR3
230338 REF

1 (COM)
3 (IN)
2 (OUT)
AR4
230337 REF

VIEW E

VIEW F

3 MOUNTING TORQUE TO BE 6 IN LBS.

2 APPLY THERMAL JOINT COMPOUND (920469) TO BOTH SURFACES OF BeO WASHER.

1 CEMENT PUSH BUTTONS TO SWITCHES AND POWER ROD

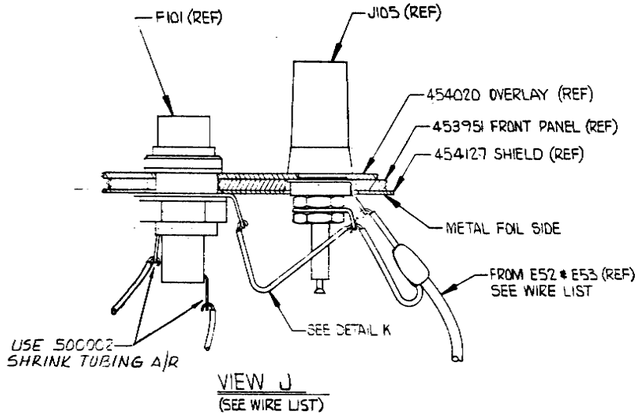
4 TO SECURE OVERLAY TO MOLDED FRONT PANEL. PROPER PREPARATION OF APPLICATION SURFACES IS ESSENTIAL TO ASSURE HIGH QUALITY, LONG LASTING APPLICATION. ASSURE ALL SURFACES TO WHICH TAPE WILL BE APPLIED ARE CONTAMINATED - (CONT. SH. 2)

NOTES: UNLESS OTHERWISE SPECIFIED

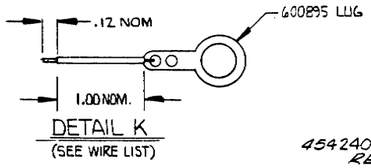
MODULE ASSY
MODEL 5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403931	S

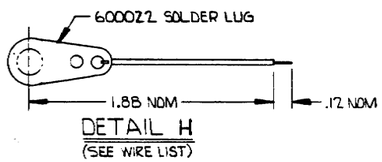
SCALE 1.0/1.5 SHEET 1 OF 2



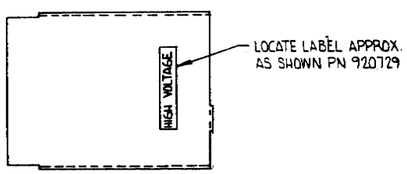
VIEW J
(SEE WIRE LIST)



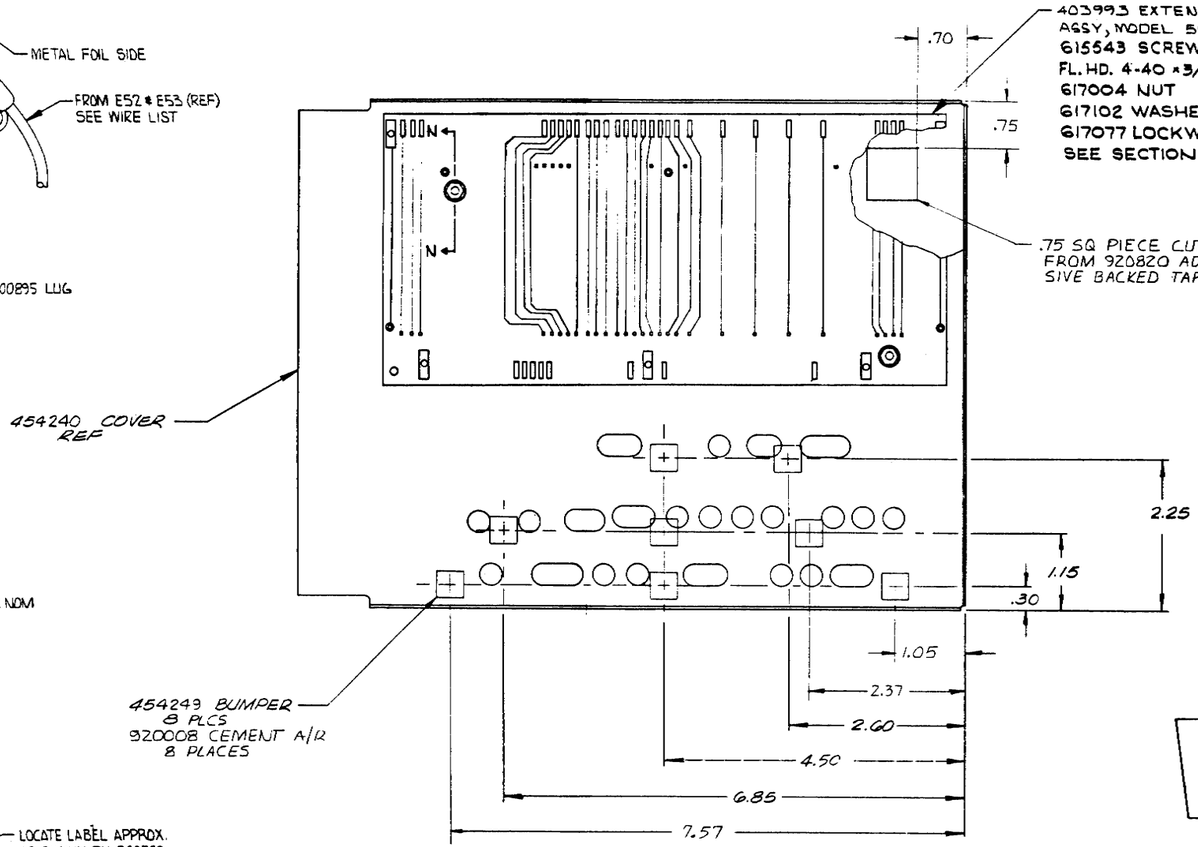
DETAIL K
(SEE WIRE LIST)



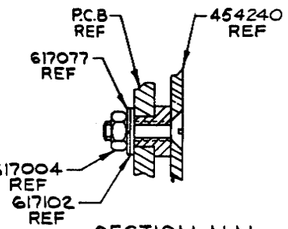
DETAIL H
(SEE WIRE LIST)



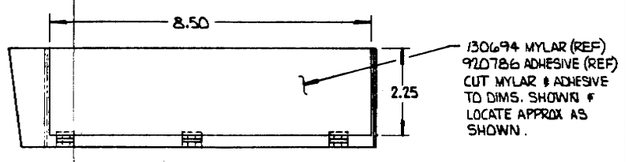
VIEW C
BOTTOM VIEW



ALL BUMPERS TO CLEAR HOLES



SECTION N-N
SCALE : NONE



VIEW P
SCALE : NONE

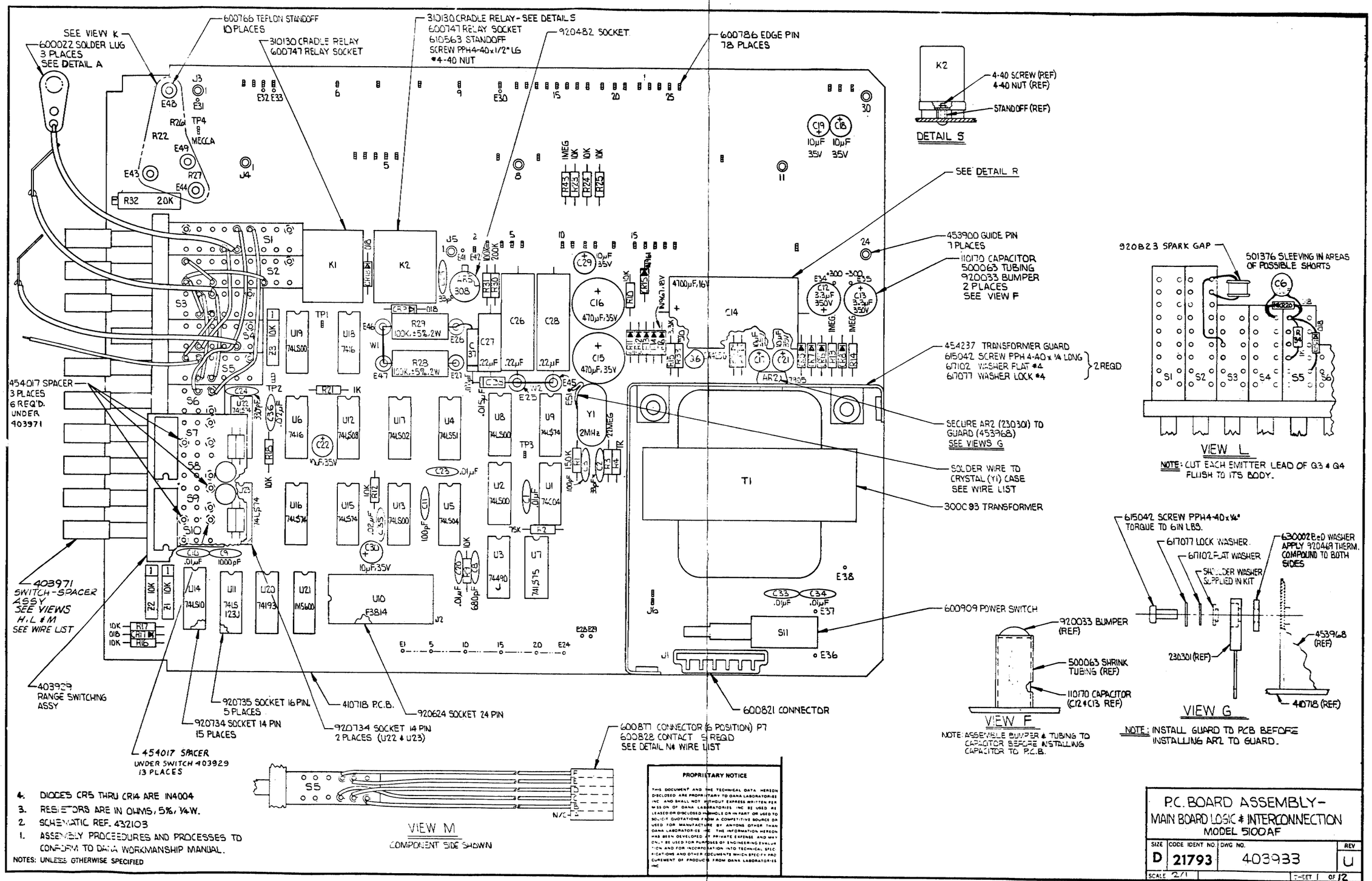
⚠ - METALS MAY BE OILY OR DUSTY; PLASTICS MAY BE COATED WITH MOLD RELEASE AGENTS, DIRT, ETC.
ANY SURFACE CONTAMINATE WILL ADVERSELY AFFECT ADHESION AND MUST BE REMOVED PRIOR TO APPLICATION BY SOLVENT WIPING.
a) WET THE APPLICATION SURFACE WITH A MILD SOLVENT SUCH AS ISOPROPYL ALCOHOL (RUBBING ALCOHOL) OR HEPTANE AND WIPE THOROUGHLY.
b) DRY THE SURFACE WITH A LINT FREE CLOTH BEFORE THE SOLVENT EVAPORATES FROM THE SURFACE.
BOND STRENGTH CAN BE IMPROVED WITH FIRM APPLICATION PRESSURE SO AS TO DEVELOP INTIMATE CONTACT OF ADHESIVE TO THE BONDING SURFACE.

NOTES: UNLESS OTHERWISE SPECIFIED

MODULE ASSY
MODEL 5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403931	S

SCALE NONE | SHEET 2 OF 3


SEE VIEW K
600022 SOLDER LUG
3 PLACES
SEE DETAIL A
600766 TEFLON STANDOFF
10 PLACES
310130 CRADLE RELAY
600747 RELAY SOCKET
310130 CRADLE RELAY - SEE DETAIL S
600747 RELAY SOCKET
610563 STANDOFF
SCREW PPH 4-40 x 1/2" LG
#4-40 NUT
920482 SOCKET
600786 EDGE PIN
78 PLACES
K2
4-40 SCREW (REF)
4-40 NUT (REF)
STANDOFF (REF)
DETAIL S
SEE DETAIL R
453900 GUIDE PIN
7 PLACES
110170 CAPACITOR
500063 TUBING
920033 BUMPER
2 PLACES
SEE VIEW F
920823 SPARK GAP
501376 SLEEVING IN AREAS OF POSSIBLE SHORTS
VIEW L
NOTE: CUT EACH EMITTER LEAD OF Q3 & Q4 FLUSH TO ITS BODY.
454237 TRANSFORMER GUARD
615042 SCREW PPH 4-40 x 1/4 LONG
617102 WASHER FLAT #4
617077 WASHER LOCK #4
2 REQD
SECURE AR2 (230301) TO GUARD (453968)
SEE VIEWS G
SOLDER WIRE TO CRYSTAL (Y1) CASE
SEE WIRE LIST
300C93 TRANSFORMER
454017 SPACER
3 PLACES
6 REQ'D.
UNDER
403971
403971
SWITCH-SPACER ASSY
SEE VIEWS H, L & M
SEE WIRE LIST
403929
RANGE SWITCHING ASSY
454017 SPACER
UNDER SWITCH 403929
13 PLACES
920735 SOCKET 16 PIN
5 PLACES
920734 SOCKET 14 PIN
15 PLACES
920734 SOCKET 14 PIN
2 PLACES (U22 & U23)
410718 P.C.B.
920624 SOCKET 24 PIN
600821 CONNECTOR
600871 CONNECTOR (6 POSITION) P7
600828 CONTACT S REQD
SEE DETAIL N & WIRE LIST
600909 POWER SWITCH
920033 BUMPER (REF)
500063 SHRINK TUBING (REF)
110170 CAPACITOR (C12 & C13 REF)
VIEW F
NOTE: ASSEMBLE BUMPER & TUBING TO CAPACITOR BEFORE INSTALLING CAPACITOR TO P.C.B.
615042 SCREW PPH 4-40 x 1/4" TORQUE TO 6 IN LBS.
617077 LOCK WASHER
617102 FLAT WASHER
SHOULDER WASHER SUPPLIED IN KIT
630002 EeD WASHER APPLY 920449 THERM. COMPOUND TO BOTH SIDES
230301 (REF)
453968 (REF)
410718 (REF)
VIEW G
NOTE: INSTALL GUARD TO PCB BEFORE INSTALLING AR2 TO GUARD.
VIEW M
COMPONENT SIDE SHOWN
4. DIODES CR5 THRU CR14 ARE IN4004
3. RESISTORS ARE IN OHMS, 5%, 1/4W.
2. SCHEMATIC REF. 432103
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.
NOTES: UNLESS OTHERWISE SPECIFIED
PROPRIETARY NOTICE
THIS DOCUMENT AND THE TECHNICAL DATA HEREON DISCLOSED ARE PROPRIETARY TO DANA LABORATORIES INC AND SHALL NOT WITHOUT EXPRESS WRITTEN PERMISSION OF DANA LABORATORIES INC BE USED RELEASED OR DISCLOSED IN WHOLE OR IN PART OR USED TO SOLICIT QUOTATIONS FROM A COMPETITIVE SOURCE OR USED FOR MANUFACTURE BY ANYONE OTHER THAN DANA LABORATORIES INC THE INFORMATION HEREON HAS BEEN DEVELOPED AT PRIVATE EXPENSE AND MAY ONLY BE USED FOR PURPOSES OF ENGINEERING EVALUATION AND FOR INCORPORATION INTO TECHNICAL SPECIFICATIONS AND OTHER DOCUMENTS WHICH SPECIFY PROCUREMENT OF PRODUCTS FROM DANA LABORATORIES INC
P.C. BOARD ASSEMBLY -
MAIN BOARD LOGIC & INTERCONNECTION
MODEL 5100AF
SIZE D
CODE IDENT NO. 21793
DWG NO. 403933
REV U
SCALE 2/1
SHEET 1 OF 12

SEE DETAIL B
SEE DETAIL C
.63
4.50
2.80
3.10
SEE DETAIL E
2.10
BLACK WIRE
WHITE WIRE
SEE VIEW J
1.80
SEE VIEW K (REF)
IF FIG. 1 IS USED INSTALL WIRE FROM E48 TO S2-B-1 ONLY.
IF FIG. 2 IS USED INSTALL WIRE FROM E48 TO S2-B-1 ONLY.
IF FIG 3 IS USED INSTALL WIRE FROM E43 TO S2-B-1 ONLY.
E30
E33
E32
E48
E31
E49
E43
E44
1.05
2.70
2.60
SEE VIEW H
SEE DETAIL D
BLK WIRE
WHITE WIRE
E35
E34
E54
SHIELD (GREEN)
E42
E41
K1
S1
S2
S3
S4
S5
2.50
3.10
5.00
3.50
SEE DETAIL F
E26
E46
E40
E39
E27
E47
E51
E45
E25
S6
4.30
S7
S8
S9
S10
SEE VIEW P FOR CONDUCTOR MODIFICATION ON CIRCUIT SIDE
E52
E53
E38
E57
E29
E28
E36
HOT MELT NOT TO EXCEED HEIGHT OF WIRE DIA.
CIRCUIT SIDE SHOWN

5002.02 TUBING EXTEND TUBING OVER EACH END OF CAPACITOR (C14) A MAX OF .06
C14
DETAIL R

SET OF ONE RESISTOR 020688	SET OF TWO RESISTORS 020688	SET OF THREE RESISTORS 020688
E48, R22, R26 9 MEG ±.01%, E49, R27 JUMPER, E43, E44	E48, R22, R26 8.99 MEG ±.1%, E49, R27 FSV, E43, E44	E48, R22 4.495M ±.1%, R26 4.495M ±.1%, E49, R27 FSV, E43, E44
FIGURE 1	FIGURE 2	FIGURE 3

.12 M (TYP)
17.20 NOM
.19 NOM (TYP)
1.00 NOM (TYP)
600022 SOLDER LUG
600394 SOLDER LUG
DETAIL D

VIEW K
COMPONENT SIDE SHOWN
(SEE SHEET 1).

.015 MIN .032 MAX. TYP
CUT EXISTING CONDUCTOR BETWEEN S8-A-1 & S8-B-1
CUT EXISTING CONDUCTOR BETWEEN S9-A-1 & S9-B-1
VIEW P
CIRCUIT SIDE SHOWN

F	03	30	E
	02	20	
	01	10	
D	03	30	C
	02	20	
	01	10	
B	03	30	A
	02	20	
	01	10	

VIEW H
S1 - S11
BOTTOM VIEW

E	03	30	F
	02	20	
	01	10	
C	03	30	D
	02	20	
	01	10	
A	03	30	B
	02	20	
	01	10	

TOP VIEW

⑩ ⑥ ⑦
⑧ ⑨ ⑤
④ ② ①
③
BOTTOM VIEW
K1 & K2
VIEW J

3.00 NOM
.12 NOM
.50 NOM
DETAIL A

.12 NOM (TYP)
.38 NOM (TYP)
WHITE WIRE
BLACK WIRE
GREEN WIRE (SHIELD)
.50 NOM
9.50 NOM
DETAIL B

.25 NOM (TYP)
.12 NOM (TYP)
2.00 NOM
DETAIL C

4.10 NOM
.25 NOM
1.50 NOM
.38 NOM
.25 NOM
2.50 NOM
4.80 NOM
DETAIL F

8.00 NOM
.12 NOM
DETAIL N
.062 BRD CONTACT SEE

AS REQUIRED SEE WIRE LIST
.12 NOM (TYP)
JUMPER PREPARATION

P.C. BOARD ASSEMBLY-
MAIN BOARD LOGIC & INTERCONNECTION
MODEL 5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403933	U

SCALE
SHEET 2 OF 12

PART OF J3 | PART OF J4 | PART OF J5

ISO OUT 17
+1V REF 18
BSC 1 — E41
LOW OUT 10
ATTEN OUT 11
DC OUT 11
+IN — J101
+10V REF 24
HV BUFF OUT 2
REF COM 25
19
KΩ SINK / EXT REF LO — J104
-IN — J102
KΩ SOURCE / EXT REF HI — J103
F101 20mA
+1V REF
REF BRIDGE GAIN OUTPUT
REF BRIDGE GAIN OUTPUT

AC S1 — K2 8 9 10
DC S2 — K1 9 8 10
KΩ S3 — K2 5 6 7
FQ S4 — 5
FILT S6
RATIO X10

R32 20K CW — 5 6
R22 E43 — R26 E48 — R27 E49 — E44
SPARK GAP 920823
R43 1M
C29 10 35V
R28 100K 2W E27 — W1 E47 — R29 100K 2W E46 — E26
C37 .033
E25 — W2 E45
C38 .015
C26 .22
C25 33pF
C28 .22
+18V
-18V
AR5 308H
R30 200K
R31 100K
C27 .22
V_{CC} K1 CR18 RD1 (2D1) 310130
V_{CC} K2 CR19 RD2 (2D1) 310130
+18V E40
E39
C6 .01
R34 1K
CR20
CR21

E42 ISO INPUT 2
AC IN 1
E30 ATTN IN 10
ATTN COM 9
HV BUFF IN 1
E31
ISO LOW 12
Q (LO) 15
PART OF J7 — REF OP AMP +IN E
REF OP AMP -IN D
+5V BS 4

HI INPUT 17
+1V REF 24
LO INPUT 16

PART OF J7 — F +1V REF; C REF BRIDGE GAIN OUTPUT; B REF BRIDGE GAIN OUTPUT

SEE SH 5
NOTES: UNLESS OTHERWISE SPECIFIED

△5
R22 JUMPER — R26 9M .01% — R27 JUMPER — E43 E48 E49 E44
CONFIGURATION A SET OF 1 RESISTOR

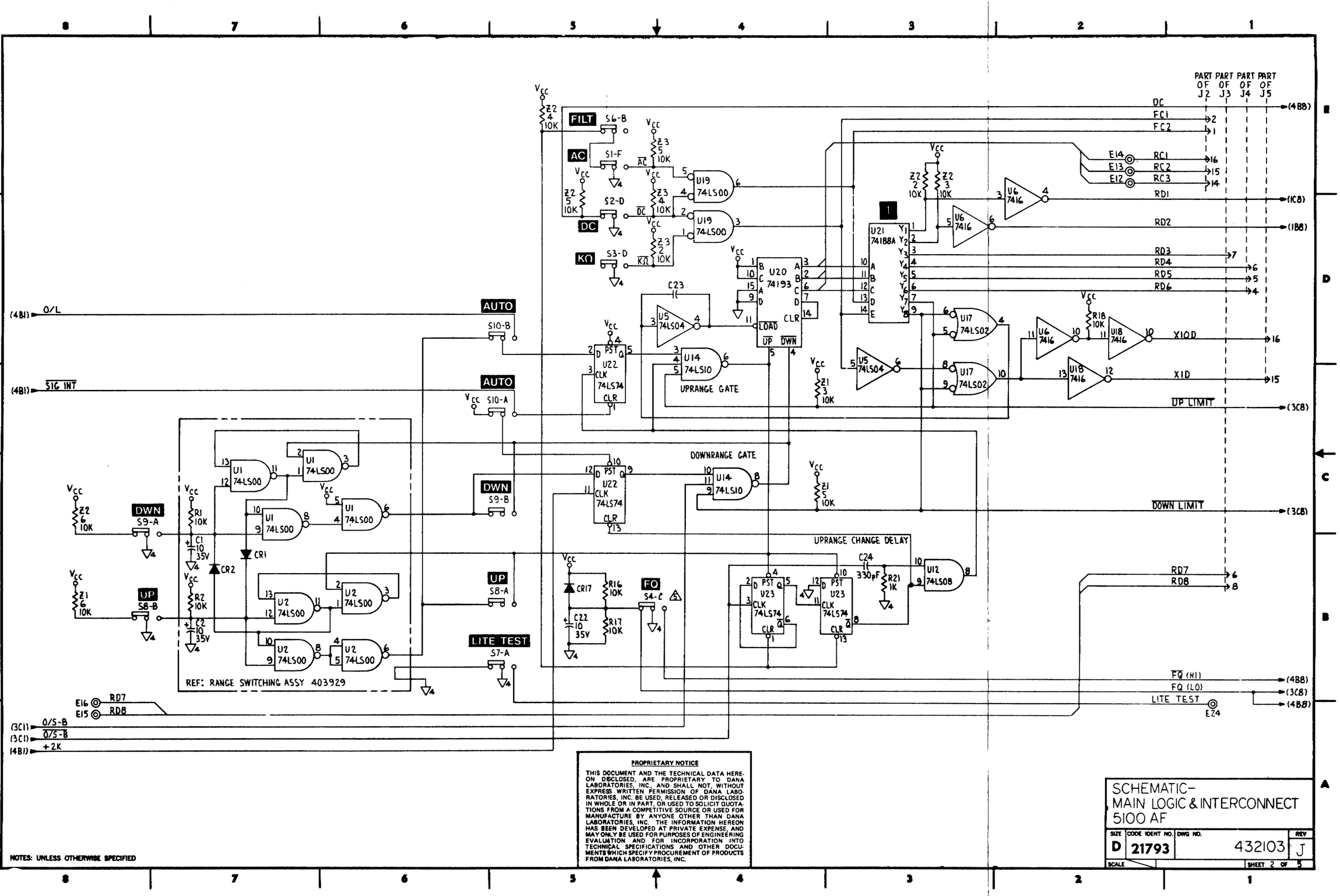
R22 JUMPER — R26 8.99M .01% — R27 FSV — E43 E48 E49 E44
CONFIGURATION B SET OF 2 RESISTORS

R22 4.495M .1% — R26 4.495M .1% — R27 FSV — E43 E48 E49 E44
CONFIGURATION C SET OF 3 RESISTORS

SCHEMATIC–
MAIN LOGIC & INTERCONNECT
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432103	J

SCALE | SHEET 1 OF 5


PART OF J2
PART OF J3
PART OF J4
PART OF J5
DC
FC1
FC2
(4B8)
E14 RC1
E13 RC2
E12 RC3
RD1
RD2
RD3
RD4
RD5
RD6
(1C8)
(1B8)
FILT
S6-B
AC
S1-F
DC
S2-D
KΩ
S3-D
U19 74LS00
U20 74193
U21 74188A
U6 7416
U17 74LS02
U18 7416
U5 74LS04
U14 74LS10
U22 74LS74
U23 74LS74
C23
C24 330pF
R18 10K
R21 1K
XIOD
XID
UP LIMIT
(3C8)
DOWN LIMIT
(3C8)
(4B1) O/L
AUTO
S10-B
(4B1) SIG INT
AUTO
S10-A
UPRANGE GATE
DOWNRANGE GATE
UPRANGE CHANGE DELAY
DWN
S9-A
DWN
S9-B
UP
S8-B
UP
S8-A
LITE TEST
S7-A
FQ
S4-C
CR1
CR2
C1 10 35V
C2 10 35V
C22 10 35V
CR17
R1 10K
R2 10K
R16 10K
R17 10K
REF: RANGE SWITCHING ASSY 403929
RD7
RD8
FQ (HI)
FQ (LO)
LITE TEST
E24
E16 RD7
E15 RD8
(3C1) O/S-B
(3C1) O/S-B
(4B1) +2K
PROPRIETARY NOTICE
THIS DOCUMENT AND THE TECHNICAL DATA HEREON DISCLOSED, ARE PROPRIETARY TO DANA LABORATORIES, INC., AND SHALL NOT, WITHOUT EXPRESS WRITTEN PERMISSION OF DANA LABORATORIES, INC. BE USED, RELEASED OR DISCLOSED IN WHOLE OR IN PART, OR USED TO SOLICIT QUOTATIONS FROM A COMPETITIVE SOURCE OR USED FOR MANUFACTURE BY ANYONE OTHER THAN DANA LABORATORIES, INC. THE INFORMATION HEREON HAS BEEN DEVELOPED AT PRIVATE EXPENSE, AND MAY ONLY BE USED FOR PURPOSES OF ENGINEERING EVALUATION AND FOR INCORPORATION INTO TECHNICAL SPECIFICATIONS AND OTHER DOCUMENTS WHICH SPECIFY PROCUREMENT OF PRODUCTS FROM DANA LABORATORIES, INC.
NOTES: UNLESS OTHERWISE SPECIFIED
SCHEMATIC-
MAIN LOGIC & INTERCONNECT
5100 AF
SIZE D
CODE IDENT NO. 21793
DWG NO. 432103
REV J
SCALE
SHEET 2 OF 5

COUNTER & CONTROL

OSC/CLK

MUX OSC

(2C1) UP LIMIT
(2C1) DOWN LIMIT
(4D1) REF INTERVAL
(2B1) FQ (LO)
(4C1) SIG INT
(4D1) INTERNAL RESET (AZ)
J2-4 HOLD
(4B1) STG INT
J202 HOLD

O/S-A (4C8)
+10 CLOCK (4D8)
O/S-B (2A8)
O/S-B (2A8) (4D8)
MUX OSC J3-6 (4D8)
PART OF J2: E18 8, E21 20, E22 10, E19 19

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC–
MAIN LOGIC & INTERCONNECT
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432103	J

SCALE — SHEET 3 OF 5

COUNTER & CONTROL

J3-29 ND

TP2

U6 7416

Z3 6 10K

R12 10K

U15 74LS74

U14 74LS10

U5 74LS04

U18 7416

AZC — PART OF J2 PART OF J3 23

(AZ) INTERNAL RESET — 20 → (3B8)

RESET — 21

U17 74LS02

U19 74LS00

U18 7416

R24 10K +10V

−RD — 13

REF INTERVAL — (3C8)

U16 74LS74

U12 74LS08

U17 74LS02

U18 7416

R23 10K +10V

+RD — 12

C30 10 +

−17V

V_{GG} MP V_{SS} TEST V_{DD} BLANK

U10 3814

(3D1) +10 CLOCK — CP

(3C1) O/S-B — TRANSFER

(3B1) MUX OSC — STEP

DP Q_{E1} Q_{E2} Q_{E2L} +2K

N_1 N_2 N_3 N_4 O_A O_B O_C O_D O_E

U13 74LS00

C11 100pF

U6 7416

C35 .02

FQ (LO) 4

FQ (HI) 13

U19 74LS00

U18 7416

R25 10K +10V

SID — 18

SIF — 19

SIG INT — (3B8)

MINUS POL — E11 — 14

PLUS POL — E10

BLANK — E20

U13 74LS00

(3D1) O/S-A

(3E1) DC

(2A1) FQ (LO)

(2B1) FQ (HI)

SIG INT — (2C8) (3B8)

O/L — (2D8)

±2K — (2A8)

O_A E5 O_B E3 O_C E2 O_D E1 O_E E4 → 3

N_1 E6 → 11

N_2 E8 → 12

N_3 E9 → 13

N_4 E7 → 17

V_{CC} V_{SS} V_{DD} V_{GG} MP TEST BLANK

PROPRIETARY NOTICE

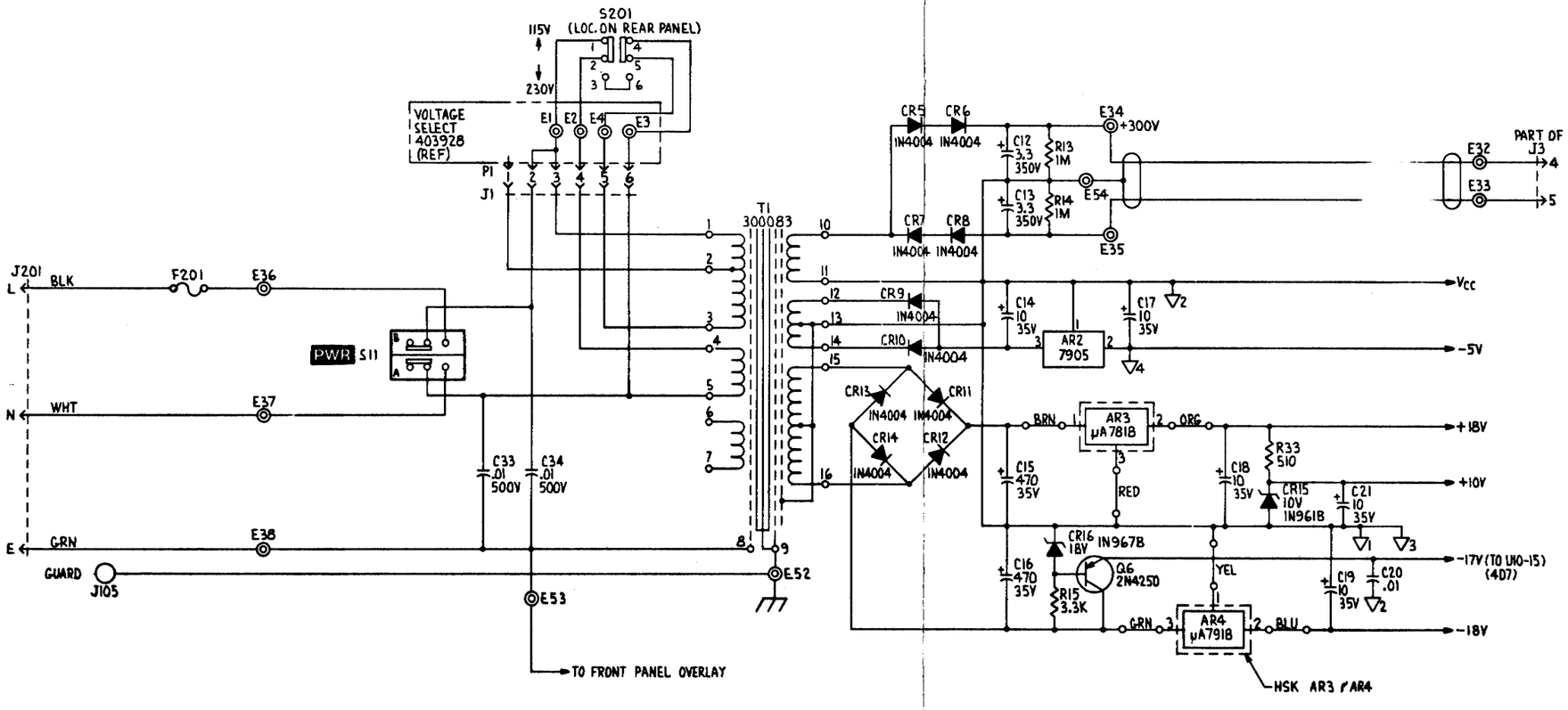
THIS DOCUMENT AND THE TECHNICAL DATA HEREON DISCLOSED, ARE PROPRIETARY TO DANA LABORATORIES, INC., AND SHALL NOT, WITHOUT EXPRESS WRITTEN PERMISSION OF DANA LABORATORIES, INC. BE USED, RELEASED OR DISCLOSED IN WHOLE OR IN PART, OR USED TO SOLICIT QUOTATIONS FROM A COMPETITIVE SOURCE OR USED FOR MANUFACTURE BY ANYONE OTHER THAN DANA LABORATORIES, INC. THE INFORMATION HEREON HAS BEEN DEVELOPED AT PRIVATE EXPENSE, AND MAY ONLY BE USED FOR PURPOSES OF ENGINEERING EVALUATION AND FOR INCORPORATION INTO TECHNICAL SPECIFICATIONS AND OTHER DOCUMENTS WHICH SPECIFY PROCUREMENT OF PRODUCTS FROM DANA LABORATORIES, INC.

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC–
MAIN LOGIC & INTERCONNECT
5100 AF

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432103	J

SCALE — SHEET 4 OF 5



POWER DISTRIBUTION							
	+18V	+10V	-18V	▽1	▽2	▽3	▽4(-5V)
J2				9			18
J3	28	14	27	3	26	30	22
J4	9		7	8		3	2
J5	13	10	11	14			3
E5	50			23			17

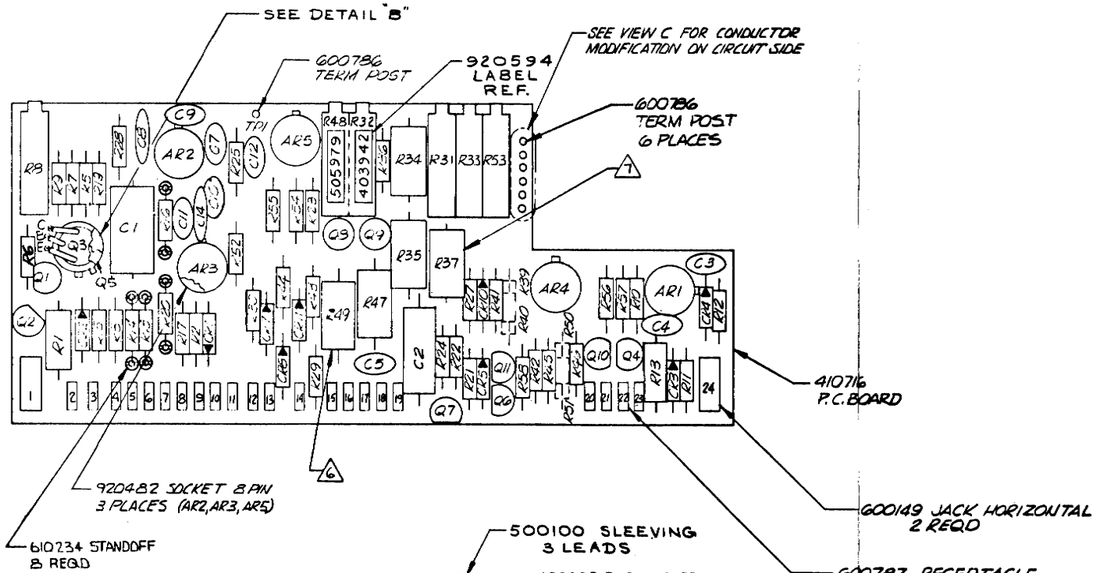
7. SYMBOL ▽1 DENOTES REF GND (MECCA)
   ▽2 ANALOG GND
   ▽3 REF GND
   ▽4 DIGITAL GND
6. R22, R26 AND R27 ARE FSV SET 020688 AND MAY BE CONFIGURED AS SHOW IN AS SHOWN A, B OR C
5. SWITCH S4 IS INOPERATIVE
4. ALL SWITCHES AND RELAYS SHOWN IN DEENERGIZED POSITION
3. DIODES ARE IN916B
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W

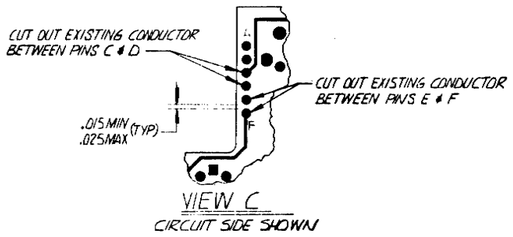
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC–
MAIN LOGIC & INTERCONNECT
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432103	J

SCALE — SHEET 5 OF 5





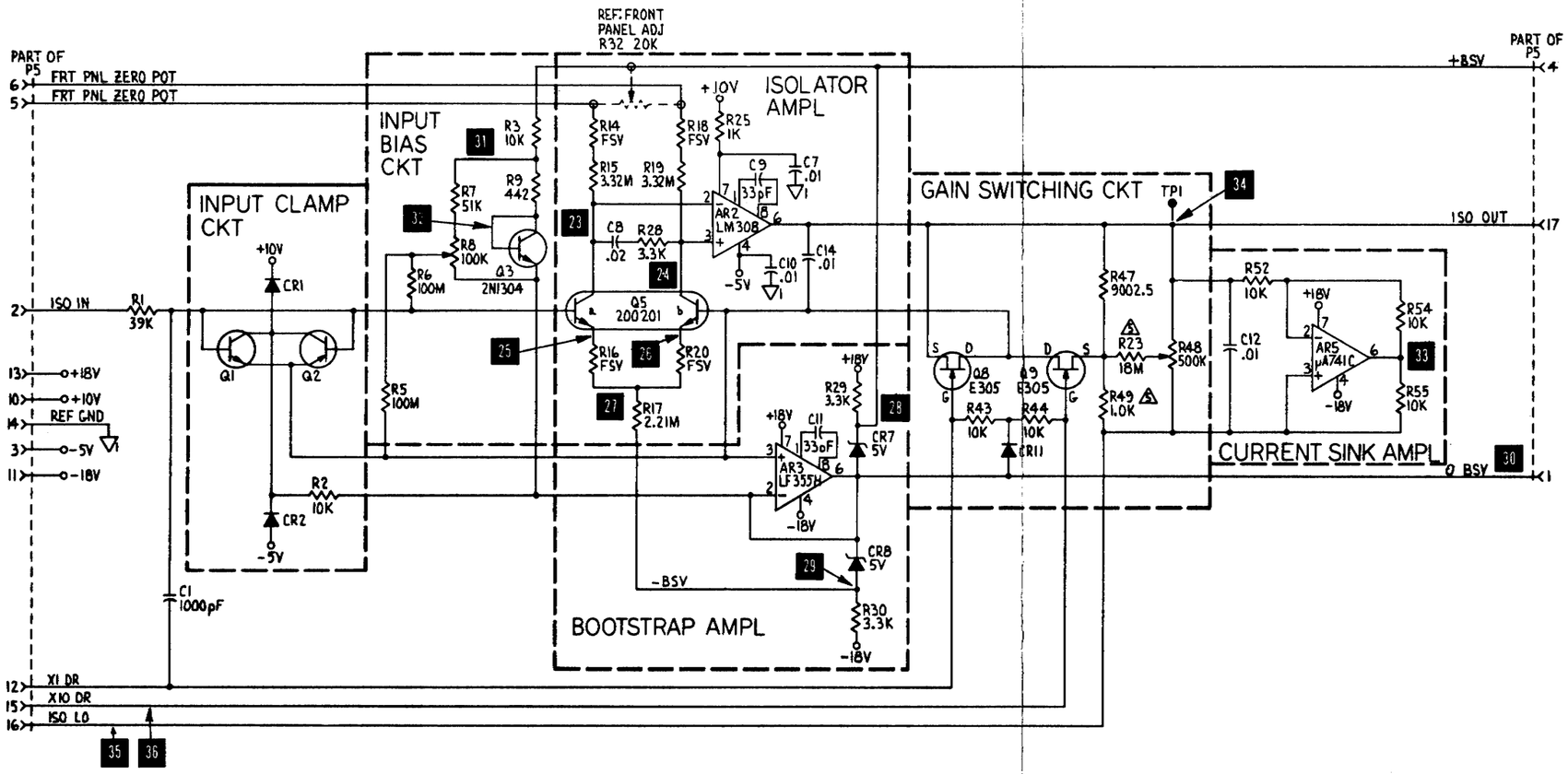
1. R34, R35 & R37 ARE A MATCHED SET 020678.
2. R47 & R49 ARE A MATCHED SET 020675.
5. INSTALL Q3 & Q5 SO THAT FIRM PHYSICAL CONTACT WITH BeO WASHER IS HELD BY HEAT SHRINKING OF TUBING. APPLY THERMOL COMPOUND TO WASHER PRIOR TO ASSEMBLY.
4. CR10, R41, R58 ARE PART OF 403942 ZENER KIT
3. SCHEMATIC REF 432104.
2. CAPACITORS ARE IN MF
1. RESISTORS ARE IN OHMS, 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

PC BOARD ASSY
REFERENCE-ISOLATOR
MODEL 5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403934	D

SCALE 2/1 SHEET 1 OF 6



⚠ ZENER REF KIT 403942
⚠ MATCHED RESISTOR SET 020678
⚠ MATCHED RESISTOR SET 020675
4. TRANSISTORS ARE 200200
3. DIODES ARE IN9168
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC–
REFERENCE ISOLATOR
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432104	C

SCALE | SHEET 1 OF 2

REFERENCE CKT

OHMS REFERENCE BUFFER AMPL

OPEN TERMINAL INPUT CLAMP CKT

OVER VOLTAGE PROTECTION CKT

REFERENCE ZENER CURRENT SINK

PART OF J7

REF BRIDGE + VOLTS → B

REF BRIDGE GAIN OUTPUT → C

PART OF P7

D REF OP AMP -IN 38

E REF OP AMP +IN 37

(KΩ)+10V REF PART OF P5 → 24

REF COM J5-19 → REF COM 20

REF BRIDGE ZENER OUT → F

+1V REF → 18

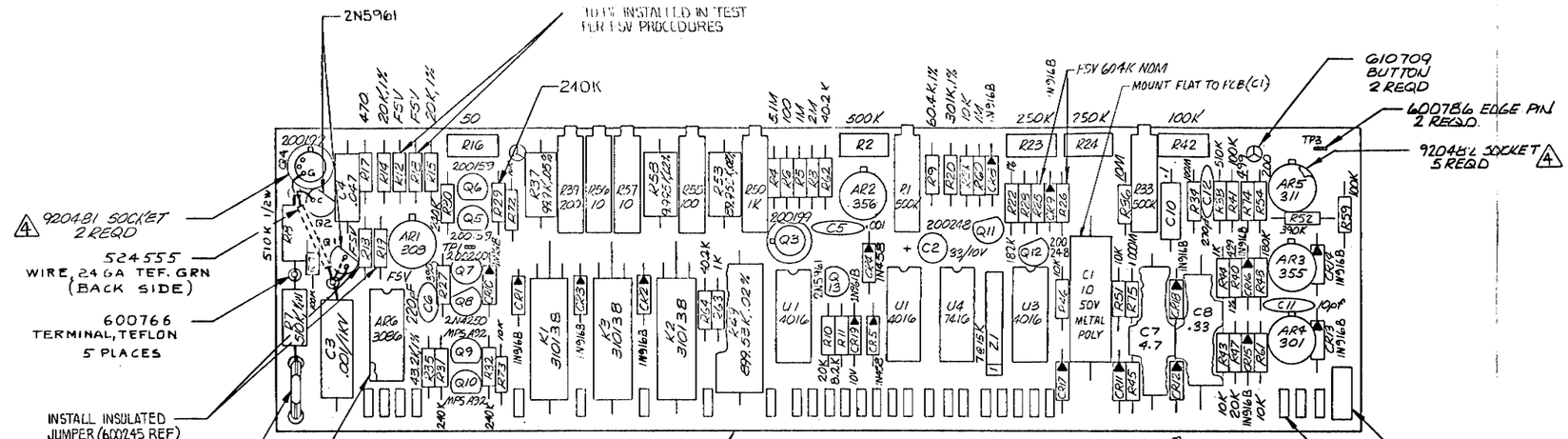
REF BRIDGE CKT SIMPLIFIED DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC-
REFERENCE ISOLATOR
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432104	C

SCALE | SHEET 2 OF 2



COMPONENT SIDE SHOWN

4 MAX. COMPONENT HEIGHTH TO BE .6 (Q3, Q4, AR1, AR2, AR3, AR4 & AR5)

3. REF SCHEMATIC 432105

2. CAPACITORS ARE IN μF

1. RESISTORS ARE IN OHMS, ±5%, 1/4W

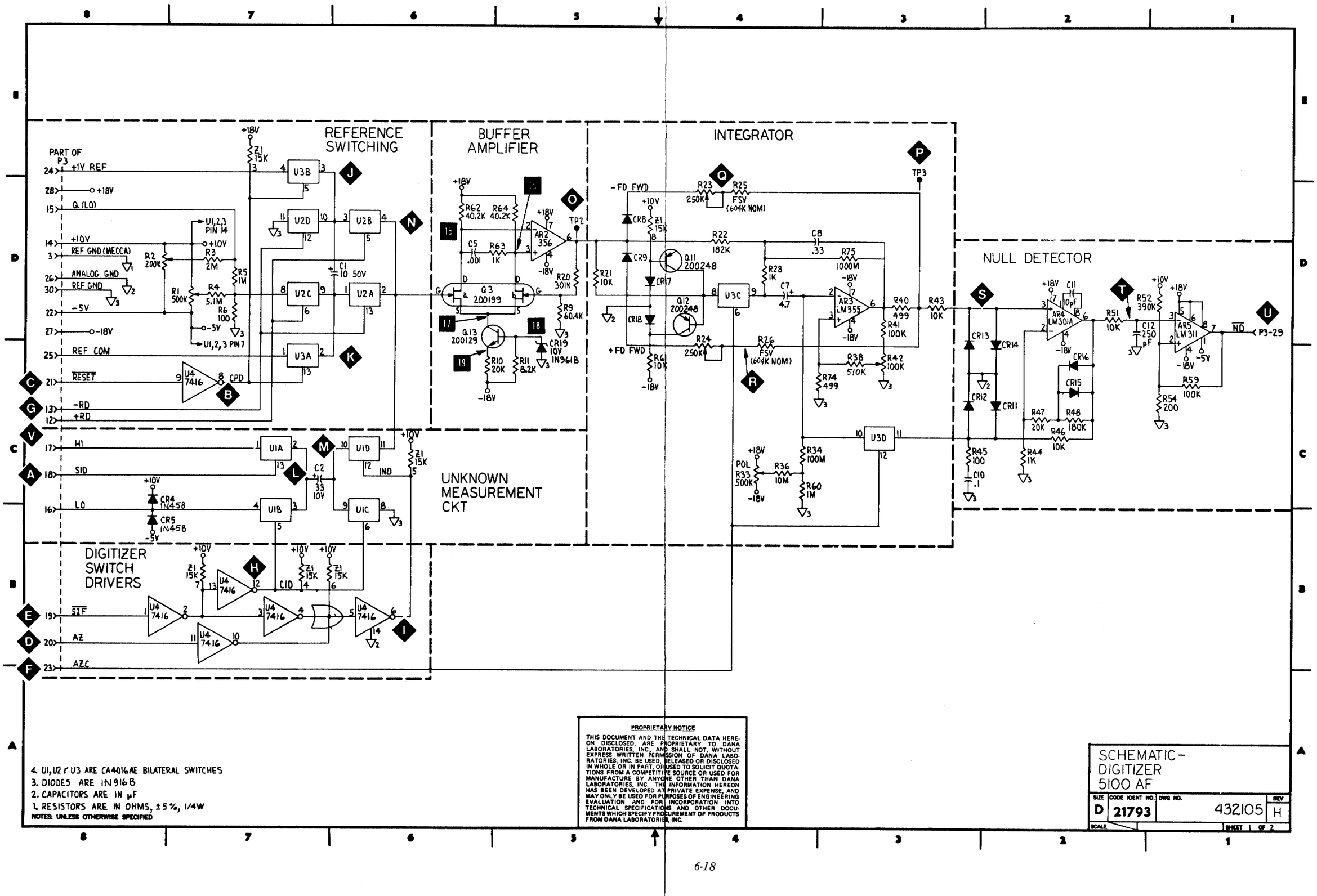
NOTES: UNLESS OTHERWISE SPECIFIED

PC BOARD ASSY
DIGITIZER
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403935	L

SCALE 2/1 SHEET 1 OF 6

6-17


REFERENCE SWITCHING
BUFFER AMPLIFIER
INTEGRATOR
NULL DETECTOR
UNKNOWN MEASUREMENT CKT
DIGITIZER SWITCH DRIVERS
PART OF P3
+1V REF
+18V
Q (LO)
+10V
REF GND (MECCA)
ANALOG GND
REF GND
-5V
-18V
REF COM
RESET
-RD
+RD
HI
SID
LO
STF
AZ
AZC
CPD
HID
LID
IND
-FD FWD
+FD FWD
POL
TP2
TP3
P3-29
PROPRIETARY NOTICE
THIS DOCUMENT AND THE TECHNICAL DATA HEREON DISCLOSED, ARE PROPRIETARY TO DANA LABORATORIES, INC., AND SHALL NOT, WITHOUT EXPRESS WRITTEN PERMISSION OF DANA LABORATORIES, INC. BE USED, RELEASED OR DISCLOSED IN WHOLE OR IN PART, OR USED TO SOLICIT QUOTATIONS FROM A COMPETITIVE SOURCE OR USED FOR MANUFACTURE BY ANYONE OTHER THAN DANA LABORATORIES, INC. THE INFORMATION HEREON HAS BEEN DEVELOPED AT PRIVATE EXPENSE, AND MAY ONLY BE USED FOR PURPOSES OF ENGINEERING EVALUATION AND FOR INCORPORATION INTO TECHNICAL SPECIFICATIONS AND OTHER DOCUMENTS WHICH SPECIFY PROCUREMENT OF PRODUCTS FROM DANA LABORATORIES, INC.
4. U1, U2 & U3 ARE CA4016AE BILATERAL SWITCHES
3. DIODES ARE IN9168
2. CAPACITORS ARE IN µF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED
SCHEMATIC – DIGITIZER 5100 AF
SIZE D
CODE IDENT NO. 21793
DWG NO. 432105
REV H
SCALE
SHEET 1 OF 2

HIGH VOLTAGE BUFFER AMPLIFIER

ATTENUATOR VOLTAGE DIVIDER

PART OF P3
ATTEN IN
+300V
HV BUFF IN
-300V
ATTEN COM
RD7
RD8
RD3

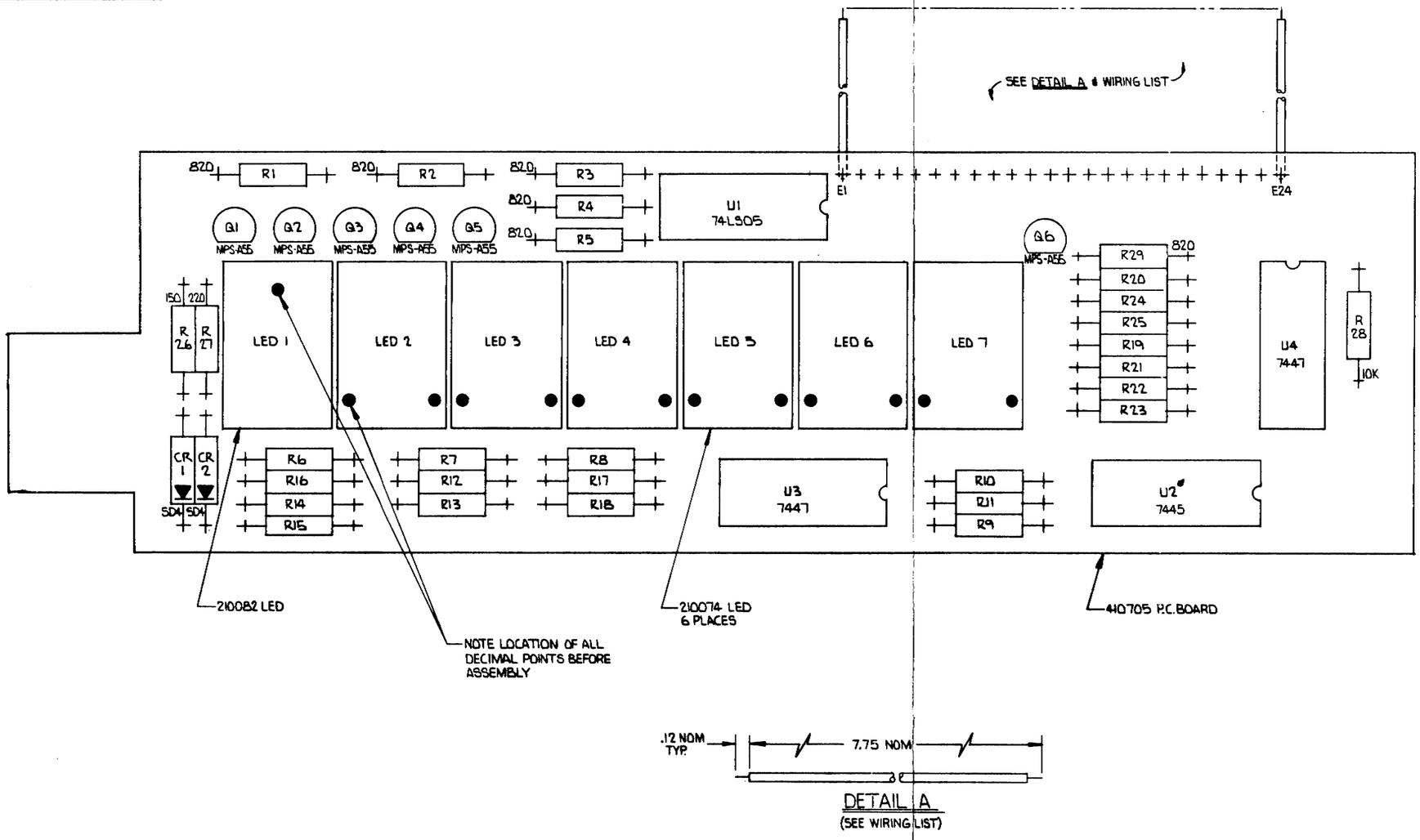
R7 510K .5W
R8 510K .5W
Q1 200129
Q2 200129
CLAMP
C3 .001
R12 FSV
R14 20K
R16 50
R15 20K
R18 FSV
R13 FSV (JUMPER NOM)
R19 FSV (JUMPER NOM)
R71 100K
C4 .047
R17 470
Q4 200199
PART OF AR6 CA3086
R35 43.2K
AR1 LM308
C6 220 pF
R72 10K
R29 240K
Q5 200159
R30 240K
Q6 200159
Q7 200200
CR10 10V IN961B
R27 390
Q8 2N4250
PART OF AR6 CA3086
Q9 MPS-A42
R31 240K
Q10 MPS-A42
R73 10K
R32 240K
TP1
PART OF P3
H.V. BUFF OUT
10M ADJ
R37 99.9K
R39 200
K1
K2
K3
R49 899.53K
R50 1K
R53 89.95K
R55 100
10V ADJ
ATTEN OUT
R57 10
1KV ADJ
R56 10
1KΩ ADJ
R58 9.995K
CR1
CR2
CR3
310138
310138
310138

AR6
CA3086
TRANSISTOR ARRAY

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC-
DIGITIZER
5100 AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432105	H
SCALE		SHEET 2 OF 2	



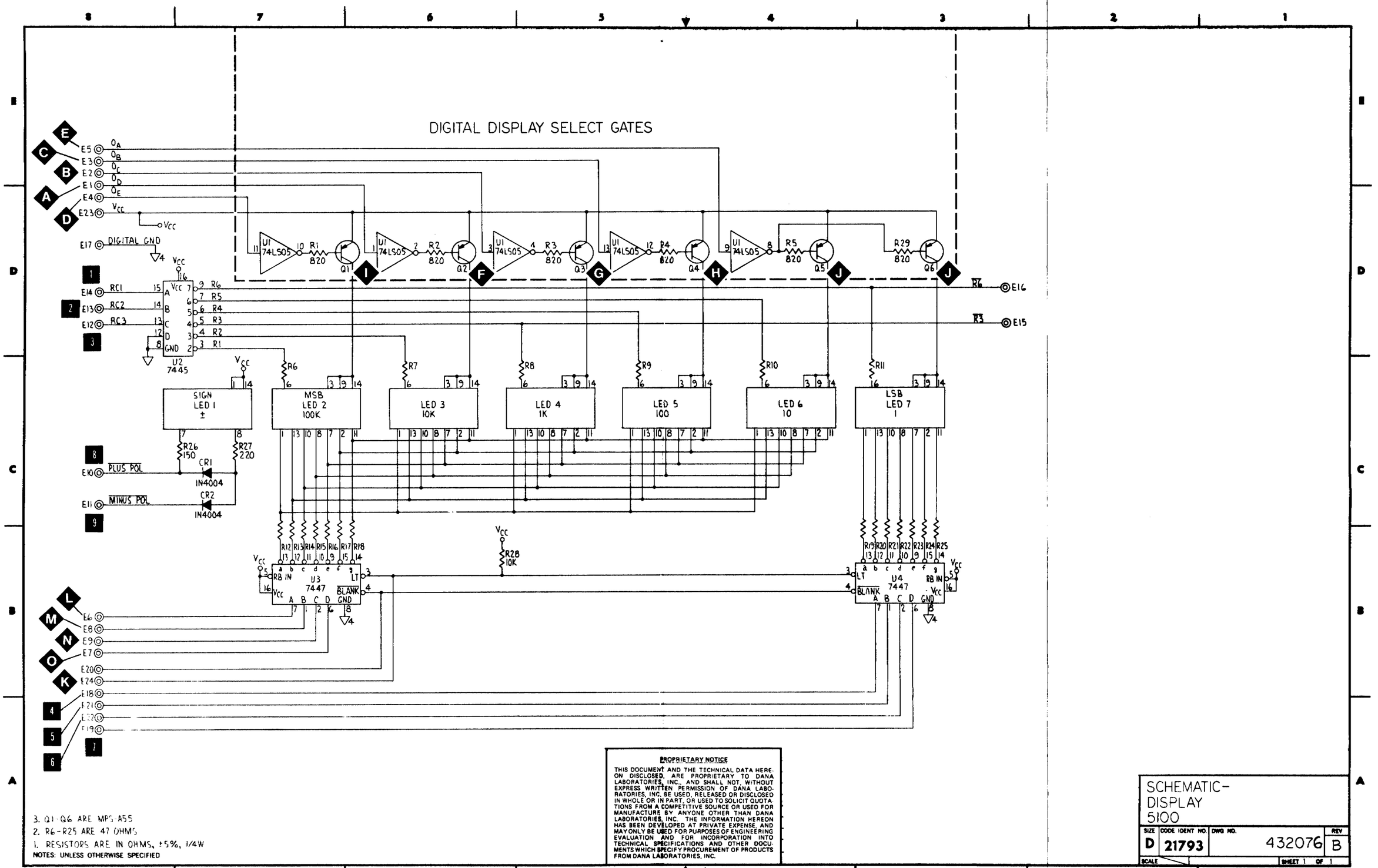
6. *FACTORY SELECT VALUE (FSV) OF ALL LED DISPLAYS ON THIS ASSEMBLY TO BE OF THE SAME LUMINOUS INTENSITY CATEGORY. LED 1 MAY BE ±1 CODE LETTER FROM LED 2 THRU LED 6.*
5. *Q1-Q6 TO BE INSTALLED MAX. .30 ABOVE P.C. BOARD*
4. R6 THRU R25 ARE 47 Ω.
3. RESISTORS ARE IN OHMS, 5%, ¼W.
2. SCHEMATIC REF. 432076.
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

DISPLAY BOARD ASSY.
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403855	D

SCALE 4/1 SHEET OF 4



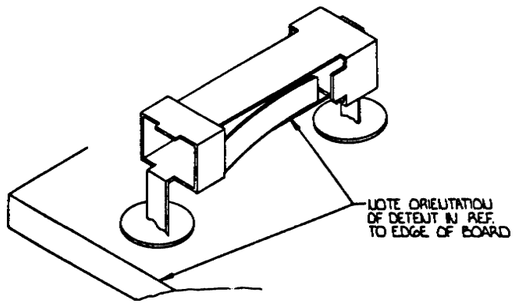
3. Q1-Q6 ARE MPS-A55
2. R6-R25 ARE 47 OHMS
1. RESISTORS ARE IN OHMS, ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

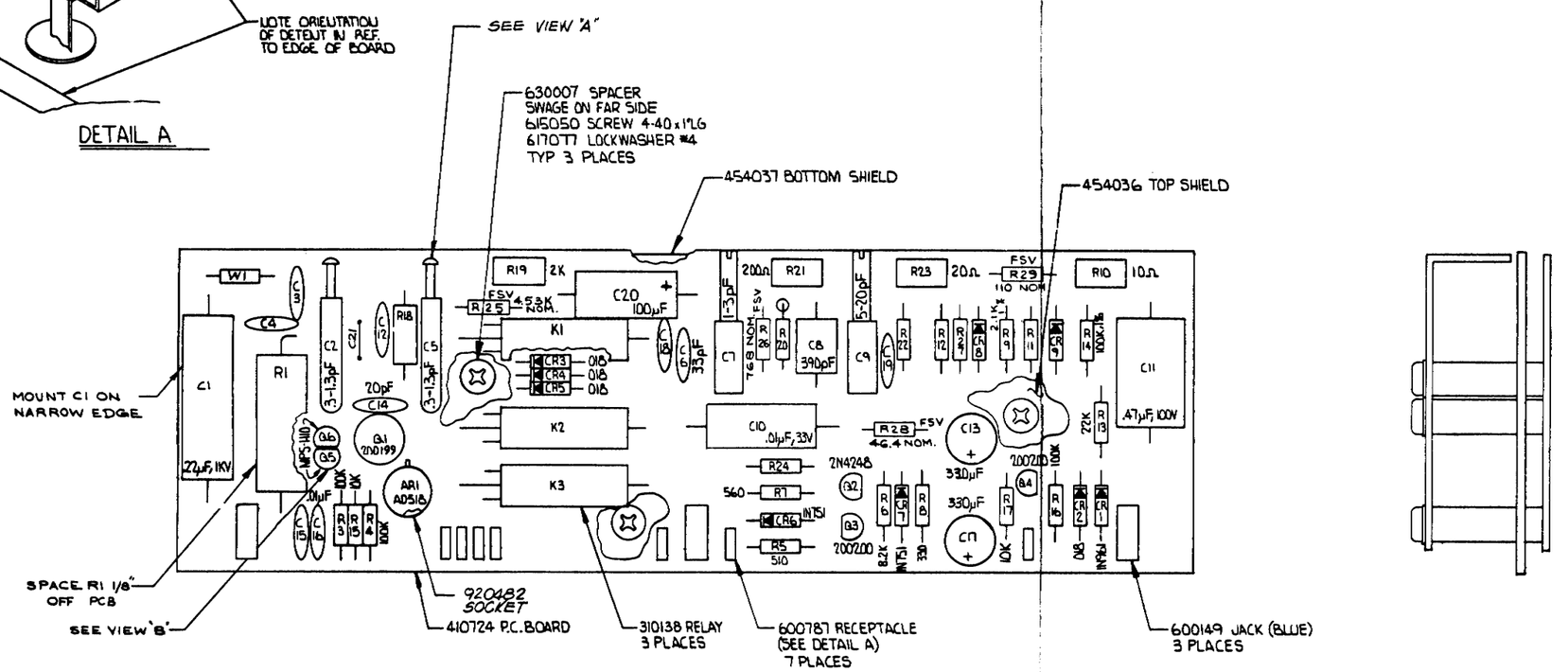
SCHEMATIC-
DISPLAY
5100

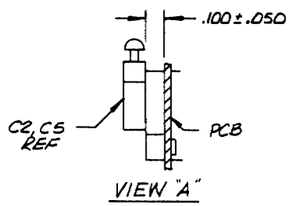
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432076	B

SCALE | SHEET 1 OF 1

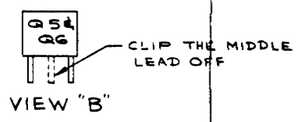


DETAIL A





VIEW "A"



VIEW "B"

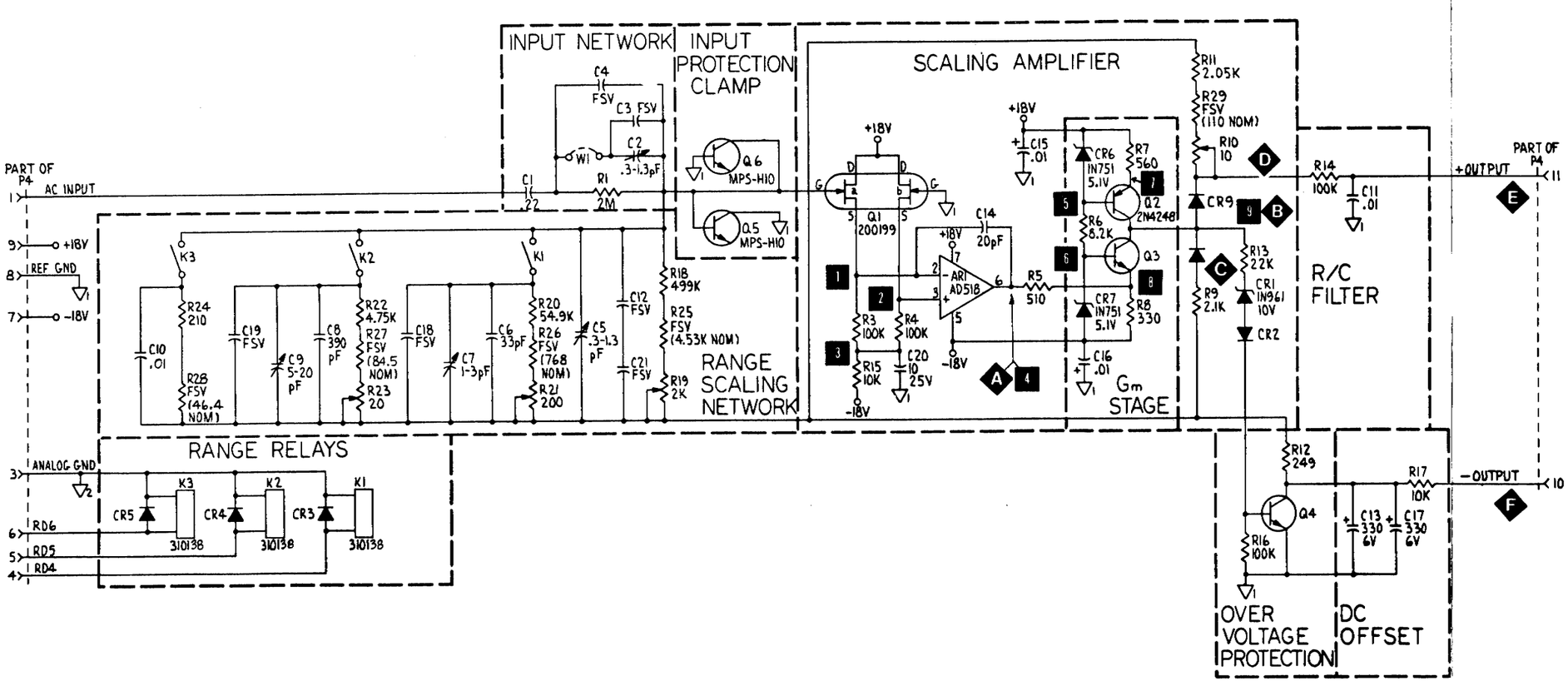
4. CUT CENTER (EMITTER) LEAD OFF ON Q5 & Q6
3. RESISTORS ARE IN OHMS, ±5%, ¼W.
2. SCHEMATIC REF. 432093.
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

P.C. BOARD ASSEMBLY
A.C. AVERAGING CONVERTER
MODEL 5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403905	P

SCALE 2/1 SHEET 1 OF 5



4. TRANSISTORS ARE 200200.
3. DIODES ARE IN916B
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W

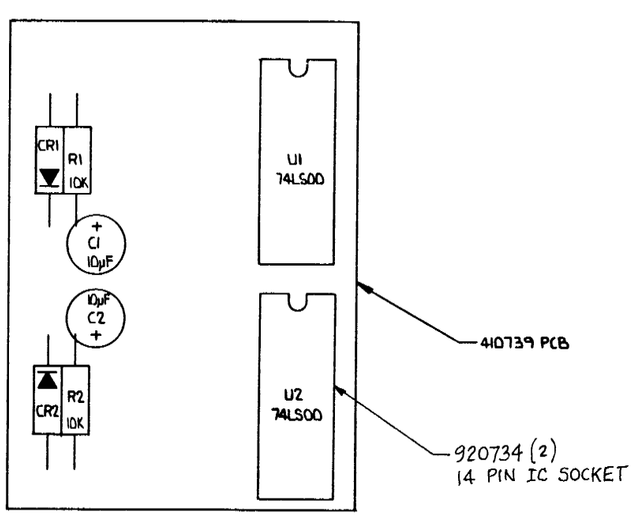
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC –
AC (AVERAGING) CONVERTER
5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432093	F

SCALE | SHEET 1 OF 1

6-23



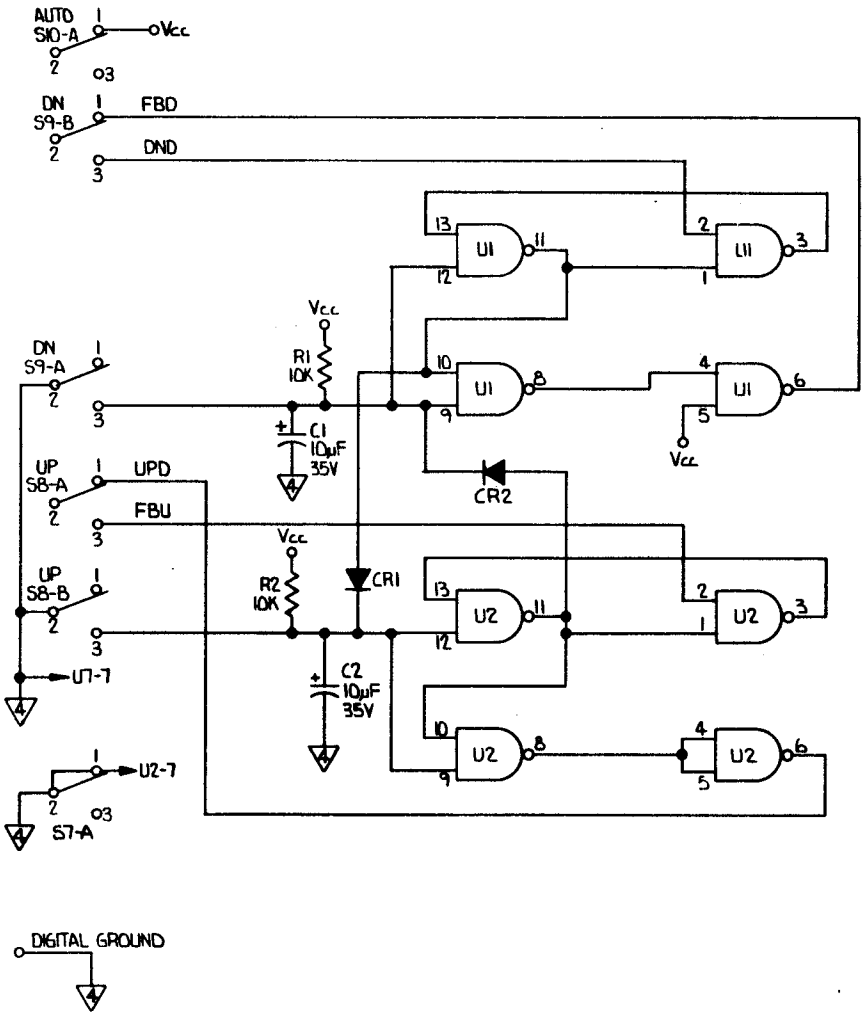
4. ALL DIODES ARE 0185.
3. ALL CAPACITORS ARE IN µF, ±20%, 35V.
2. ALL RESISTORS ARE IN OHMS, ±5%, 1/4W.
1. SCHEMATIC REFERENCE 432101.

NOTES: UNLESS OTHERWISE SPECIFIED

RANGE SWITCHING ASSY.
5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403929	B

SCALE 4/1 SHEET 1 OF 2



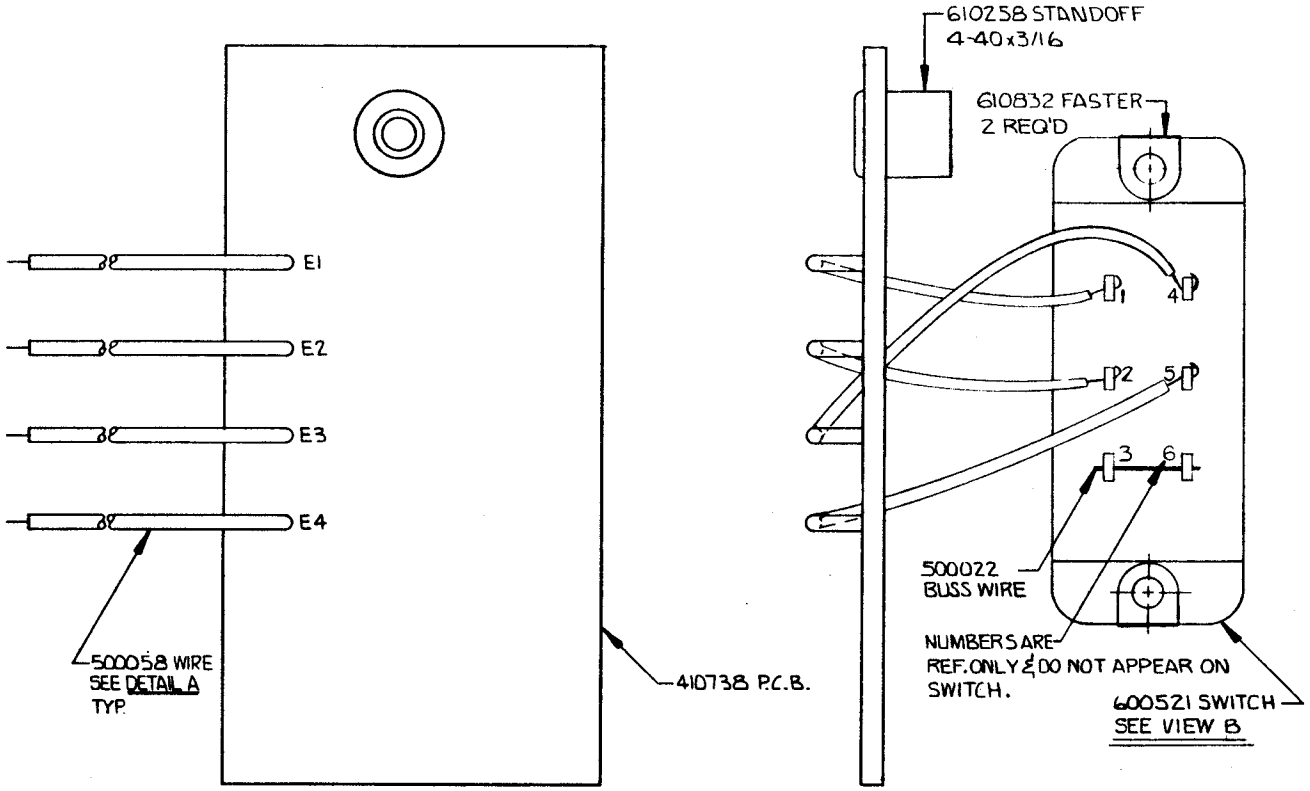
3. ALL RESISTORS ARE IN OHMS, ±5%, ¼W.
2. ALL DIODES ARE 018.
1. U1 & U2 ARE 74LS00.

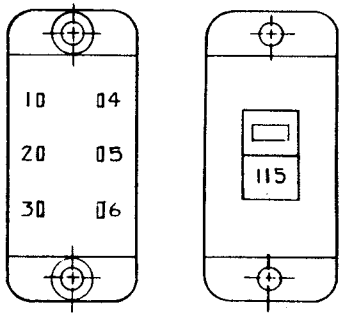
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC-
RANGE SWITCHING
5100AF

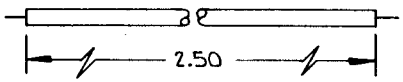
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	432101	A

SCALE NONE | SHEET | OF





VIEW B



DETAIL A

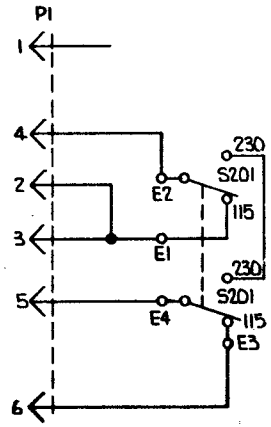
VOLTAGE SELECT ASSY.
5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403928	C

SCALE 4/1 SHEET 1 OF 2

1. SCHEMATIC REFERENCE 432100.

NOTES: UNLESS OTHERWISE SPECIFIED



NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC-
VOLTAGE SELECT
5100AF

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	432100	A

SCALE NONE SHEET OF

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

7.2 Manufacturers are identified by FSC numbers listed in table 7.2, "List of Suppliers." The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

7.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 7.1 along with the commercial equivalent.

Table 7.2 - List of Suppliers

FSC	NAME	FSC	NAME
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN	04713	MOTOROLA, INC. (Semi-Conductor Products Div.) PHOENIX, ARIZONA
01297	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS	05245	CORCOM, INC. CHICAGO, ILLINOIS
03888	PYROFILM CORP. WHIPPANY, NEW JERSEY	05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO
04222	AEROVOX CORP. (Hi-Q Division) MYRTLE BEACH, SOUTH CAROLINA	07263	FAIRCHILD (Semiconductor Division) MOUNTAIN VIEW, CALIFORNIA

Table 7.2 - List of Suppliers continued

FSC	NAME
07716	TRW ELECTRONIC COMPONENTS (IRC) BURLINGTON, IOWA
08257	NPC ELECTRONICS CANOGA PARK, CALIFORNIA
09023	CORNELL-DUBILIER ELECTRONICS SANFORD, NORTH CAROLINA
11236	CTS OF BERNE, INC. BERNE, INDIANA
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
12406	ELPAC, INC. IRVINE, CALIFORNIA
13571	ELECTRONIC RESEARCH CO. OVERLAND PARK, KANSAS
14752	ELECTRO CUBE, INC. SAN GABRIEL, CALIFORNIA
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CALIFORNIA
22045	JORDAN ELECTRIC CO. VAN NUYS, CALIFORNIA
26625	MIAL USA, INC. NUTLEY, NEW JERSEY
26806	AMERICAN ZETTLER, INC. COSTA MESA, CALIFORNIA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
32293	INTERSIL, INC. CUPERTINO, CALIFORNIA
34553	AMPEREX/MEPCO-ELECTRA (Component Division) ST. PAUL, MINNESOTA
50434	HEWLETT-PACKARD CO. (HPA Division) PALO ALTO, CALIFORNIA
52763	STETTNER-TRUSH CAZENOVIA, NEW YORK
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71707	COTO-COIL CO., INC. PROVIDENCE, RHODE ISLAND
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, LONG ISLAND, NEW YORK
74970	E. F. JOHNSON CO. WASECA, MINNESOTA
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
80294	BOURNS, INC. RIVERSIDE, CALIFORNIA
81349	MILITARY SPECIFICATION
83330	HERMAN H. SMITH, INC. BROOKLYN, NEW YORK
86884	RCA (Electronics Components Division) HARRISON, NEW JERSEY
91637	DALE ELECTRONICS, INC. COLUMBUS, NEBRASKA

403931 – Assy., MODULE, 5100AF

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
AR3	230338	INTEGRATED CIRCUIT				07263	μA7818UC
AR4	230337	INTEGRATED CIRCUIT				07263	μA7918UC
C40	100046	CAP CERAM	.01 MFD	1 KV	20%	56289	C023B102K103M
F201	920802	FUSE, SLO BLOW	.25 AMP	250 V		75915	213.250
F101	920800	FUSE, FAST ACTING	1/50 AMP	250 V		75915	211.020
	403855	PCB ASSY, DISPLAY				21793	403855
	403905	PCB ASSY, AC AVERAGING CONVERTER				21793	403905
	403928	VOLTAGE SELECTOR ASSY				21793	403928
	403933	PCB ASSY, MAIN LOGIC & INTERCONNECTION				21793	403933
	403934	PCB ASSY, REFERENCE ISOLATOR				21793	403934
	403935	PCB ASSY, DIGITIZER				21793	403935
	403993	EXTENDER BOARD ASSY				21793	403993
J101	600908	POST, BINDING, BLACK				83330	1517-103
J102	600908	POST, BINDING, BLACK				83330	1517-103
J103	600907	POST, BINDING, WHITE				83330	1517-101
J104	600907	POST, BINDING, WHITE				83330	1517-101
J105	600908	POST, BINDING, BLACK				83330	1517-103
J201	310137	FILTER, RFI POWER	1 AMP•	115-250 V		05245	1EF1

403933 – Assy., PCB, MAIN LOGIC & INTERCONNECT, 5100AF

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
AR2	230301	INTEGRATED CIRCUIT					04713	MC7905CP
AR5	230103	INTEGRATED CIRCUIT					27014	LM308
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C3	101145	CAP	CERAM	100 PFD	500 V	10%	04222	TCD-DI-1N5600-100
C6	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
C8	100126	CAP	CERAM	680 PFD	1 KV	20%	56289	C023B102E681M
C9	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C11	101145	CAP	CERAM	100 PFD	500 V	10%	04222	TCD-DI-1N5600-100
C12	110170	CAP	ELECT	3.3 MFD	350 V	10%		350VB3.3
C13	110170	CAP	ELECT	3.3 MFD	350 V	10%		350VB3.3
C14	110185	CAP	ELECT	4700 MFD	16 V			16TAL4700
C15	110172	CAP	ELECT	470 MFD	35 V			35VBSL470
C16	110172	CAP	ELECT	470 MFD	35 V			35VBSL470
C17	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C18	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C19	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C20	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C21	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C22	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C23	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
C24	100124	CAP	CERAM	330 PFD	1 KV	20%	56289	C023B102E331M
C25	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C26	120349	CAP	POLY	.22 MFD	200 V	5%	14752	950B1C224J
C27	120290	CAP	MYLAR	.22 MFD	100 V	20%	73445	C281AH/A220K
C28	120349	CAP	POLY	.22 MFD	200 V	5%	14752	950B1C224J
C29	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C30	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C33	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
C34	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
C35	100068	CAP	CERAM	.02 MFD	100 V	20%	56289	C023B101H203M
C36	100068	CAP	CERAM	.02 MFD	100 V	20%	56289	C023B101H203M
C37	121091	CAP	MYLAR	.033 MFD	100 V	10%	09023	WMF1S33
C38	121090	CAP	MYLAR	.015 MFD	100 V	10%	09023	WMF1S15
CR5	210004	DIODE	SILICO				81349	1N4004
CR6	210004	DIODE	SILICO				81349	1N4004
CR7	210004	DIODE	SILICO				81349	1N4004
CR8	210004	DIODE	SILICO				81349	1N4004
CR9	210004	DIODE	SILICO				81349	1N4004

403933 – Assy., PCB, MAIN LOGIC & INTERCONNECT, 5100AF *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR10	210004	DIODE SILICO	81349	1N4004
CR11	210004	DIODE SILICO	81349	1N4004
CR12	210004	DIODE SILICO	81349	1N4004
CR13	210004	DIODE SILICO	81349	1N4004
CR14	210004	DIODE SILICO	81349	1N4004
CR15	220004	DIODE SILICO ZENER	81349	1N961B
CR16	220015	DIODE SILICO ZENER	81349	1N967B
CR17	211083	DIODE SILICO	81349	1N916B
CR18	211083	DIODE SILICO	81349	1N916B
CR19	211083	DIODE SILICO	81349	1N916B
CR20	211083	DIODE SILICO	81349	1N916B
CR21	211083	DIODE SILICO	81349	1N916B
J1	600821	CONN 6 P	27264	09-03-1062
K1	310130	RELAY 2 FORM C 1 KV CONTACT 5 V COIL	26806	AZ-420-217-200
K2	310130	RELAY 2 FORM C 1 KV CONTACT 5 V COIL	26806	AZ-420-217-200
Q6	200068	TRANS PNP	80131	2N4250
R1	000154	RES CARBON 150 K 5% 1/4W	81349	RC07GF154J
R2	000753	RES CARBON 75 K 5% 1/4W	81349	RC07GF753J
R3	000226	RES CARBON 22 M 5% 1/4W	81349	RC07GF226J
R4	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R9	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R10	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R12	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R13	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R14	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R15	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R16	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R17	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R18	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R21	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R22	020688	RES SET, PRECISION	21793	020688
R23	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R24	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J

403933 – Assy., PCB, MAIN LOGIC & INTERCONNECT, 5100AF *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R25	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R26	020688	RES SET, PRECISION	21793	020688
R27	020688	RES SET, PRECISION	21793	020688
R28	030005	RES CARBON 100 K 5% 2 W	81349	RC42GF104J
R29	030005	RES CARBON 100 K 5% 2 W	81349	RC42GF104J
R30	000204	RES CARBON 200 K 5% 1/4W	81349	RC07GF204J
R31	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R32	040304	POT CERMET 20 K 10%	91637	784 Series
R33	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R34	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R43	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
S1-S10	403974	SWITCH SPACER ASSY	21793	403974
S11	600909	SWITCH, PUSHBUTTON	21793	600909
T1	300093	TRANS POWER	21793	300093
U1	230195	INTEGRATED CIRCUIT	27014	CMOS74C04N
U2	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U3	230348	INTEGRATED CIRCUIT, CERAMIC	01295	SN74490J
U4	230196	INTEGRATED CIRCUIT	01295	SN74LS51N
U5	230234	INTEGRATED CIRCUIT	01295	SN74LS04N
U6	230108	INTEGRATED CIRCUIT	01295	SN7416N
U7	230354	INTEGRATED CIRCUIT	07263	74LS75
U8	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U9	230350	INTEGRATED CIRCUIT	07263	74LS74
U10	230120	INTEGRATED CIRCUIT	07263	3814
U11	230347	INTEGRATED CIRCUIT, CERAMIC	01295	SN74LS123J
U12	230351	INTEGRATED CIRCUIT	07263	74LS08
U13	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U14	230248	INTEGRATED CIRCUIT	01295	SN74LS10N
U15	230350	INTEGRATED CIRCUIT	07263	74LS74
U16	230350	INTEGRATED CIRCUIT	07263	74LS74
U17	230352	INTEGRATED CIRCUIT	07263	74LS02
U18	230108	INTEGRATED CIRCUIT	01295	SN7416N
U19	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U20	230353	INTEGRATED CIRCUIT	07263	74193
U21	230300	INTEGRATED CIRCUIT ROM	32293	IM5600C-PE
U22	230350	INTEGRATED CIRCUIT	07263	74LS74
U23	230350	INTEGRATED CIRCUIT	07263	74LS74

403933 – Assy., PCB, MAIN LOGIC & INTERCONNECT, 5100AF *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Y1	920599	CRYSTAL 2.0 MHz	13571	
Z1	080005	RES NETWORK CERMET 10 K 6P,5R 2%	11236	750-61-R10KΩ
Z2	080005	RES NETWORK CERMET 10 K 6P,5R 2%	11236	750-61-R10KΩ
Z3	080005	RES NETWORK CERMET 10 K 6P,5R 2%	11236	750-61-R10KΩ
	403929	RANGE SWITCHING ASSY	21793	403929

403929 – Assy., RANGE SWITCHING

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C2	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
CR1	211083	DIODE	SILICO				81349	1N916B
CR2	211083	DIODE	SILICO				81349	1N916B
U1	230193	INTEGRATED CIRCUIT					01295	SN74LS00N
U2	230193	INTEGRATED CIRCUIT					01295	SN74LS00N
R1	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R2	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J

403855 – Assy., PCB, DISPLAY, MODEL 5100

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR1	210004	DIODE SILICO	81349	1N4004
CR2	210004	DIODE SILICO	81349	1N4004
LED 1	210082	DIODE LED DISPLAY	50434	HP5082-7662
LED 2	210074	DIODE LED DISPLAY 7 SEG YELLOW	50434	HP5082-7660
LED 3	210074	DIODE LED DISPLAY 7 SEG YELLOW	50434	HP5082-7660
LED 4	210074	DIODE LED DISPLAY 7 SEG YELLOW	50434	HP5082-7660
LED 5	210074	DIODE LED DISPLAY 7 SEG YELLOW	50434	HP5082-7660
LED 6	210074	DIODE LED DISPLAY 7 SEG YELLOW	50434	HP5082-7660
LED 7	210074	DIODE LED DISPLAY 7 SEG YELLOW	50434	HP5082-7660
Q1	200184	TRANS PNP	04713	MPSA55
Q2	200184	TRANS PNP	04713	MPSA55
Q3	200184	TRANS PNP	04713	MPSA55
Q4	200184	TRANS PNP	04713	MPSA55
Q5	200184	TRANS PNP	04713	MPSA55
Q6	200184	TRANS PNP	04713	MPSA55
R1	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R2	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R3	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R4	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R5	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R6	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R7	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R8	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R9	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R10	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R11	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R12	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R13	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R14	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R15	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R16	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R17	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R18	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R19	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R20	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R21	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R22	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R23	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J

403855 – Assy., PCB, DISPLAY, MODEL 5100 *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R24	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R25	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R26	000151	RES CARBON 150 OHM 5% 1/4W	81349	RC07GF151J
R27	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R28	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R29	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
U1	230192	INTEGRATED CIRCUIT	01295	SN74LS05N
U2	230071	INTEGRATED CIRCUIT	07263	7445
U3	230132	INTEGRATED CIRCUIT	07263	7447
U4	230132	INTEGRATED CIRCUIT	07263	7447

403935 – Assy., PCB, DIGITIZER, 5100AF

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
AR1	230103	INTEGRATED CIRCUIT					27014	LM308
AR2	230324	INTEGRATED CIRCUIT					27014	LF356H
AR3	230331	INTEGRATED CIRCUIT					27014	LF355H
AR4	230110	INTEGRATED CIRCUIT					27014	LM301A
AR5	230307	INTEGRATED CIRCUIT					27014	LM311H
AR6	230118	INTEGRATED CIRCUIT					86884	CA3086
C1	120347	CAP	POLY	10.0 MFD	50 V	20%	14752	650B1A106
C2	110159	CAP	TANTA	33 MFD	10 V	10%	05397	T368B336K010AS
C3	120184	CAP	POLY	1000 PFD	1 KV	5%	26625	611
C4	120321	CAP	MYLAR	.047 MFD	250 V	10%	73445	C281AB/A47K
C5	100071	CAP	CERAM	.001 MFD	1 KV	20%	56289	C023B102E102M
C6	100088	CAP	CERAM	220 PFD	100 V	5%	72982	8121-M100-C0G221J
C7	120335	CAP	POLY	4.7 MFD	63 V	10%	52763	MKC1860-547/06
C8	120341	CAP		33 MFD	200 V	10%	07716	X363
C10	120286	CAP	MYLAR	.1 MFD	100 V	20%	73445	C281AH/A100K
C11	100125	CAP	CERAM	10 PFD	1 KV	20%	56289	C023B102E100M
C12	100120	CAP	CERAM	270 PFD	1 KV	20%	56289	C023B102E271M
CR1	211083	DIODE	SILICO				81349	1N916B
CR2	211083	DIODE	SILICO				81349	1N916B
CR3	211083	DIODE	SILICO				81349	1N916B
CR4	210058	DIODE	SILICO				81349	1N458
CR5	210058	DIODE	SILICO				81349	1N458
CR8	211083	DIODE	SILICO				81349	1N916B
CR9	211083	DIODE	SILICO				81349	1N916B
CR10	220004	DIODE	SILICO	ZENER			81349	1N961B
CR11	211083	DIODE	SILICO				81349	1N916B
CR12	211083	DIODE	SILICO				81349	1N916B
CR13	211083	DIODE	SILICO				81349	1N916B
CR14	211083	DIODE	SILICO				81349	1N916B
CR15	211083	DIODE	SILICO				81349	1N916B
CR16	211083	DIODE	SILICO				81349	1N916B
CR17	211083	DIODE	SILICO				81349	1N916B
CR18	211083	DIODE	SILICO				81349	1N916B
CR19	220004	DIODE	SILICO	ZENER			81349	1N961B
K1	310138	RELAY	REED				71707	CR-4551
K2	310138	RELAY	REED				71707	CR-4551
K3	310138	RELAY	REED				71707	CR-4551

403935 – Assy., PCB, DIGITIZER, 5100AF *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q1	200129	TRANS SILICO NPN	81349	2N5961
Q2	200129	TRANS SILICO NPN	81349	2N5961
Q3	200199	TRANS FET	27014	FM1302
Q4	200199	TRANS FET	27014	FM1302
Q5	200159	TRANS SILICO NPN	21793	200159
Q6	200159	TRANS SILICO NPN	21793	200159
Q7	200200	TRANS NPN	21793	200200
Q8	200068	TRANS PNP	80131	2N4250
Q9	200198	TRANS PNP	04713	MPS-A92
Q10	200198	TRANS PNP	04713	MPS-A92
Q11	200248	TRANS SPECIAL PURPOSE, MODIFIED	21793	200248
Q12	200248	TRANS SPECIAL PURPOSE, MODIFIED	21793	200248
Q13	200129	TRANS SILICO NPN	81349	2N5961
R1	040238	POT CERMET 500 K 10% 3/4W	73138	89PR500K
R2	040266	POT CERMET 500 K 20% 1/2W	73138	72XW500K
R3	000205	RES CARBON 2 M 5% 1/4W	81349	RC07GF205J
R4	000515	RES CARBON 5.1 M 5% 1/4W	81349	RC07GF515J
R5	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R6	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R7	001887	RES CARBON 510 K 5% 1/2W	81349	RC20GF514J
R8	001887	RES CARBON 510 K 5% 1/2W	81349	RC20GF514J
R9	010013	RES METAL 60.4 K T-2 1% 1/8W	81349	RN60C6042F
R10	010392	RES METAL 20 K .1% 1/10W	81349	RN55C2002B
R11	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R12	001737	RES CARBON FSV 5% 1/4W	21793	001737
R13	600245	JUMPER, INSULATED		L-2007-1LP
R14	010639	RES METAL 20 K .1% 1/10W	81349	RN55E2002B
R15	010639	RES METAL 20 K .1% 1/10W	81349	RN55E2002B
R16	040257	POT CERMET 50 OHM 20% 1/2W	80294	3389S-500
R17	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R18	001737	RES CARBON FSV 5% 1/4W	21793	001737
R19	600245	JUMPER, INSULATED		L-2007-1LP
R20	012025	RES METAL 301 K 1% 1/8W	81349	RN60C3013F
R21	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R22	010208	RES METAL 182 K T-0 1% 1/8W	81349	RN60D1823F
R23	040182	POT CERMET 250 K 20% 1/2W	11237	360S254B
R24	040182	POT CERMET 250 K 20% 1/2W	11237	360S254B
R25	010467	RES METAL FSV 1% 1/8W	21793	010467
R26	010467	RES METAL FSV 1% 1/8W	21793	010467
R27	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J

403935 – Assy., PCB, DIGITIZER, 5100AF *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R28	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R29	000244	RES	CARBON	240 K	5% 1/4W	81349	RC07GF244J
R30	000244	RES	CARBON	240 K	5% 1/4W	81349	RC07GF244J
R31	000244	RES	CARBON	240 K	5% 1/4W	81349	RC07GF244J
R32	000244	RES	CARBON	240 K	5% 1/4W	81349	RC07GF244J
R33	040238	POT	CERMET	500 K	10% 3/4W	73138	89PR500K
R34	000107	RES	CARBON	100 M	5% 1/4W	81349	RC07GF107J
R35	010818	RES	METAL	43.2 K	1% 1/10W	81349	RN55C4322F
R36	000106	RES	CARBON	10 M	5% 1/4W	81349	RC07GF106J
R37	020676	RES	WW	99.9 K	.02%	21793	020676
R38	000514	RES	CARBON	510 K	5% 1/4W	81349	RC07GF514J
R39	040227	POT	CERMET	200 OHM	10% 3/4W	73138	89PR200
R40	010918	RES	METAL	499 OHM	1% 1/10W	81349	RN55C4990F
R41	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R42	040210	POT	CERMET	100 K	2% 1 W	11237	360S104B
R43	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R44	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R45	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R46	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R47	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R48	000184	RES	CARBON	180 K	5% 1/4W	81349	RC07GF184J
R49	020677	RES	WW	ATTENUATOR SET		21793	020677
R50	040229	POT	CERMET	1 K	10% 3/4W	73138	89PR1K
R51	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R52	000394	RES	CARBON	390 K	5% 1/4W	81349	RC07GF394J
R53	020677	RES	WW	ATTENUATOR SET		21793	020677
R54	000201	RES	CARBON	200 OHM	5% 1/4W	81349	RC07GF201J
R55	040226	POT	CERMET	100 OHM	10% 3/4W	73138	89PR100
R56	040240	POT	CERMET	10 OHM	20% 3/4W	73138	89PR10
R57	040240	POT	CERMET	10 OHM	20% 3/4W	73138	89PR10
R58	020677	RES	WW	ATTENUATOR SET		21793	020677
R59	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R60	000105	RES	CARBON	1 M	5% 1/4W	81349	RC07GF105J
R61	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R62	010541	RES	METAL	40.2 K	1% 1/10W	81349	RN55C4022F
R63	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R64	010541	RES	METAL	40.2 K	1% 1/10W	81349	RN55C4022F
R71	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R72	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R73	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R74	010918	RES	METAL	499 OHM	1% 1/10W	81349	RN55C4990F
R75	000108	RES	CARBON	1000 M	20% 1/4W	01121	CB1082

403935 – Assy., PCB, DIGITIZER, 5100AF *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
U1	230313	INTEGRATED CIRCUIT	86884	CD4016AE
U2	230313	INTEGRATED CIRCUIT	86884	CD4016AE
U3	230313	INTEGRATED CIRCUIT	86884	CD4016AE
U4	230108	INTEGRATED CIRCUIT	01295	SN7416N
Z1	080012	RES NETWORK CERMET 15 K 8P,7R 2%	11236	750-81-R15KΩ

403934 – Assy., PCB, REFERENCE ISOLATOR

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
AR1	230085	INTEGRATED CIRCUIT					27014	LM308AH
AR2	230103	INTEGRATED CIRCUIT					27014	LM308
AR3	230331	INTEGRATED CIRCUIT					27014	LF355H
AR4	230299	INTEGRATED CIRCUIT					27014	LM312H
AR5	230119	INTEGRATED CIRCUIT			μA741		07263	741HC
C1	120004	CAP	POLY	.001 MFD	500 V	5%	08257	KSO Series
C2	120344	CAP	POLY	.1 MFD	400 V	20%	12406	ZD4A104M
C3	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C4	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C8	100068	CAP	CERAM	.02 MFD	100 V	20%	56289	C023B101H203M
C9	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C11	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	211083	DIODE	SILICO				81349	1N916B
CR2	211083	DIODE	SILICO				81349	1N916B
CR3	210004	DIODE	SILICO				81349	1N4004
CR4	220078	DIODE	SELECTED	ZENER	5 V	5%	81349	1N5231
CR5	220078	DIODE	SELECTED	ZENER	5 V	5%	81349	1N5231
CR7	220078	DIODE	SELECTED	ZENER	5 V	5%	81349	1N5231
CR8	220078	DIODE	SELECTED	ZENER	5 V	5%	81349	1N5231
CR10	403942	ZENER REFERENCE KIT					21793	403942
CR11	211083	DIODE	SILICO				81349	1N916B
Q1	200129	TRANS	SILICO	NPN			81349	2N5961
Q2	200068	TRANS		PNP			80131	2N4250
Q3	201084	TRANS	GERMAN	PNP			81349	2N1304
Q4	200246	TRANS	GRADED	MPS-A92			21793	200246
Q5	200201	TRANS	DUAL	NPN			21793	200201
Q6	200200	TRANS		NPN			21793	200200
Q7	200129	TRANS	SILICO	NPN			81349	2N5961
Q8	200230	TRANS	FET	N-CHAN, SIL JUNCTION				E305
Q9	200230	TRANS	FET	N-CHAN, SIL JUNCTION				E305
Q10	200200	TRANS		NPN			21793	200200

403934 – Assy., PCB, REFERENCE ISOLATOR *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
Q11	200200	TRANS		NPN		21793	200200
R1	001889	RES	CARBON	39 K	5% 1/2W	81349	RC20GF393J
R2	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R3	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R5	000107	RES	CARBON	100 M	5% 1/4W	81349	RC07GF107J
R6	012039	RES	PF	100 M	5%	03888	Type PVC60
R7	000513	RES	CARBON	51 K	5% 1/4W	81349	RC07GF513J
R8	040235	POT	CERMET	100 K	10% 3/4W	73138	89PR100K
R9	012008	RES	METAL	442 OHM	1% 1/10W	81349	RN55C4420F
R10	000332	RES	CARBON	3.3 K	5% 1/4W	81349	RC07GF332J
R11	000153	RES	CARBON	15 K	5% 1/4W	81349	RC07GF153J
R12	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R13	001766	RES	CARBON	220 K	5% 1/2W	81349	RC20GF224J
R14	001737	RES	CARBON	FSV	5% 1/4W	21793	001737
R15	012013	RES	C/M FOIL	3.32 M	1% 1/4W	01121	CC3324F
R16	600245	JUMPER, INSULATED					L-2007-1LP
R17	012009	RES	C/M FOIL	2.21 M	1% 1/4W	01121	CC2214F
R18	001737	RES	CARBON	FSV	5% 1/4W	21793	001737
R19	012013	RES	C/M FOIL	3.32 M	1% 1/4W	01121	CC3324F
R20	600245	JUMPER, INSULATED					L-2007-1LP
R21	000683	RES	CARBON	68 K	5% 1/4W	81349	RC07GF683J
R22	000364	RES	CARBON	360 K	5% 1/4W	81349	RC07GF364J
R23	000186	RES	CARBON	18 M	5% 1/4W	81349	RC07GF186J
R24	000513	RES	CARBON	51 K	5% 1/4W	81349	RC07GF513J
R25	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R27	000224	RES	CARBON	220 K	5% 1/4W	81349	RC07GF224J
R28	000332	RES	CARBON	3.3 K	5% 1/4W	81349	RC07GF332J
R29	000332	RES	CARBON	3.3 K	5% 1/4W	81349	RC07GF332J
R30	000332	RES	CARBON	3.3 K	5% 1/4W	81349	RC07GF332J
R31	040226	POT	CERMET	100 OHM	10% 3/4W	73138	89PR100
R32	040227	POT	CERMET	200 OHM	10% 3/4W	73138	89PR200
R33	040226	POT	CERMET	100 OHM	10% 3/4W	73138	89PR100
R34	020678	RES	WW	REF GAIN SET		21793	020678
R35	020678	RES	WW	REF GAIN SET		21793	020678
R36	001759	RES	CARBON	5.1 OHM	5% 1/4W	81349	RC07GF5R1J
R37	020678	RES	WW	REF GAIN SET		21793	020678
R39	001737	RES	CARBON	FSV	5% 1/4W	21793	001737
R40	001737	RES	CARBON	FSV	5% 1/4W	21793	001737

403934 – Assy., PCB, REFERENCE ISOLATOR *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R41	403942	ZENER REFERENCE KIT	21793	403942
R42	020693	RES WW 1 K .1%	22045	J-90
R43	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R44	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R45	001737	RES CARBON FSV 5% 1/4W	21793	001737
R46	001737	RES CARBON FSV 5% 1/4W	21793	001737
R47	020675	RES WW ISOLATOR GAIN	21793	020675
R48	040238	POT CERMET 500 K 10% 3/4W	73138	89PR500K
R49	020675	RES WW ISOLATOR GAIN	21793	020675
R50	001737	RES CARBON FSV 5% 1/4W	21793	001737
R51	001737	RES CARBON FSV 5% 1/4W	21793	001737
R52	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R53	040235	POT CERMET 100 K 10% 3/4W	73138	89PR100K
R54	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R55	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R56	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R57	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R58	403942	ZENER REFERENCE KIT	21793	403942

403942 – Assy., ZENER REFERENCE KIT

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
CR1	220082	DIODE	REF	ZENER		04713	Z483
R1	020689	RES	WW	FSV		21793	020689
R2	001737	RES	CARBON	FSV	5% 1/4W	21793	001737

403905 – Assy., PCB, AC AVERAGING CONVERTER, OPTION 14

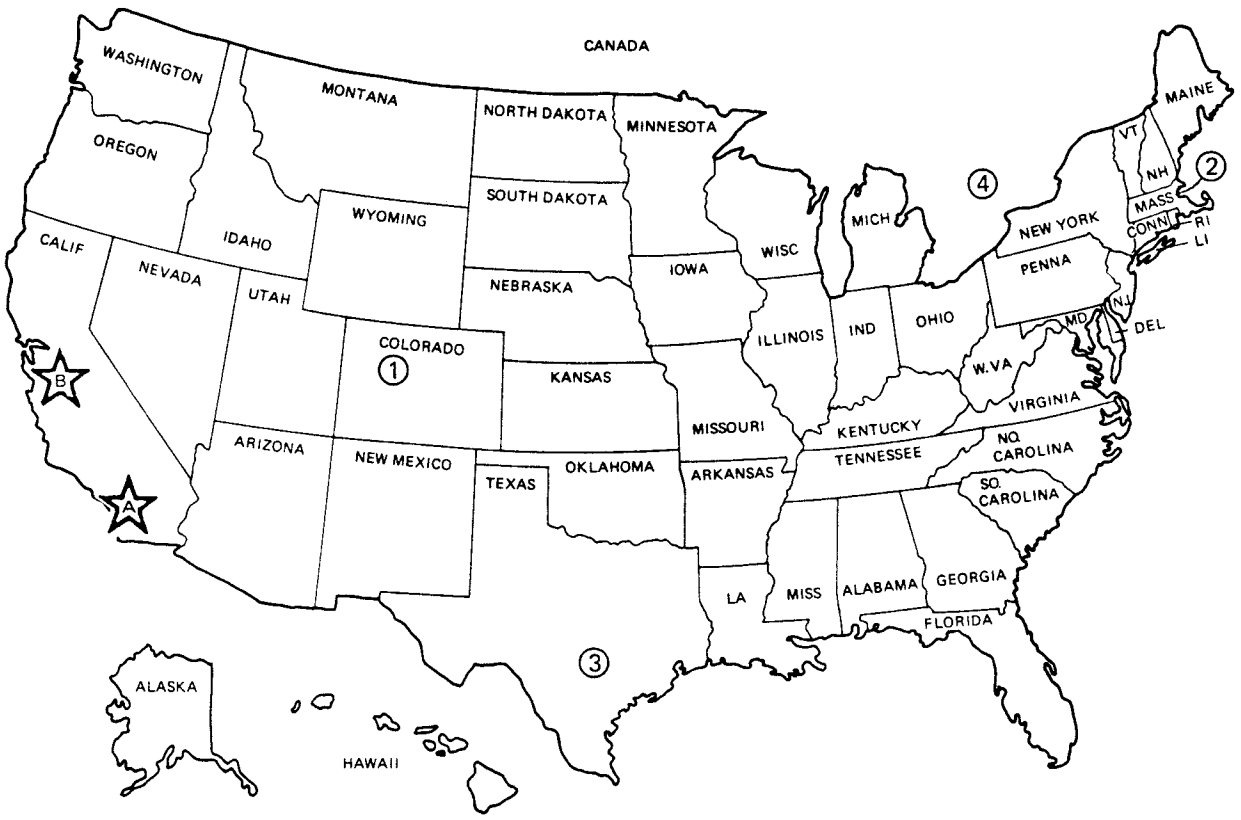
REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
AR1	230180	INTEGRATED CIRCUIT					27014	LM318H
C1	120280	CAP	MYLAR	.22 MFD	1000 V	10%	27556	ZA2J224K
C2	130146	CAP	TRIMMER	.25-1.5 PFD			74970	273-0001-002
C3	100100	CAP	CERAM	FSV			21793	100100
C4	100100	CAP	CERAM	FSV			21793	100100
C5	130146	CAP	TRIMMER	.25-1.5 PFD			74970	273-0001-002
C6	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C7	130123	CAP	TRIMMER	1-3 PFD	250 V		52763	R-TRIK0-122-09SD
C8	120158	CAP	POLY	390 PFD	63 V	5%	26625	611
C9	130148	CAP	TRIMMER	5-20 PFD	250 V		52763	R-TRIK0-122-09MG
C10	120246	CAP	POLY	0.01 MFD	33 V	5%	08257	KSC Series
C11	120294	CAP	MYLAR	.47 MFD	100 V	20%	73445	C281AH/A470K
C12	100100	CAP	CERAM	FSV			21793	100100
C13	110186	CAP	TANTA	330 MFD	6 V		05397	T362D337K006AS
C14	100076	CAP	CERAM	20 PFD	1000 V	5%	56289	C030B102F200J
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C16	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C17	110186	CAP	TANTA	330 MFD	6 V		05397	T362D337K006AS
C18	100100	CAP	CERAM	FSV			21793	100100
C19	100100	CAP	CERAM	FSV			21793	100100
C20	111148	CAP	ELECT	100 MFD	25 V		34553	ET101X025A5
C21	600245	JUMPER INSULATED						L-2007-1LP
CR1	220004	DIODE	SILICO	ZENER			81349	1N961B
CR2	211083	DIODE	SILICO				81349	1N916B
CR3	211083	DIODE	SILICO				81349	1N916B
CR4	211083	DIODE	SILICO				81349	1N916B
CR5	211083	DIODE	SILICO				81349	1N916B
CR6	220007	DIODE	SILICO	ZENER			81349	1N751A
CR7	220007	DIODE	SILICO	ZENER			81349	1N751A
CR8	210015	DIODE					50434	HP5082-2800
CR9	210015	DIODE					50434	HP5082-2800
K1	310138	RELAY	REED				71707	CR-4551
K2	310138	RELAY	REED				71707	CR-4551
K3	310138	RELAY	REED				71707	CR-4551
Q1	200199	TRANS	FET				27014	FM1302
Q2	200088	TRANS	SILICO	PNP			80131	2N4248
Q3	200200	TRANS		NPN			21793	200200
Q4	200200	TRANS		NPN			21793	200200

403905 – Assy., PCB, AC AVERAGING CONVERTER, OPTION 14 *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q5	200197	TRANS	SILICO	NPN			04713	MPS-H10
Q6	200197	TRANS	SILICO	NPN			04713	MPS-H10
R1	012041	RES	MF	2 M	T-9	.1%	03888	PME70
R3	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R4	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R5	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R6	000822	RES	CARBON	8.2 K		5% 1/4W	81349	RC07GF822J
R7	000561	RES	CARBON	560 OHM		5% 1/4W	81349	RC07GF561J
R8	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R9	010929	RES	METAL	2.10 K		1% 1/10W	81349	RN55C2101F
R10	040255	POT	CERMET	10 OHM		20% 1/2W	73138	72XW10
R11	012042	RES	MF	2.05 K	T-9	.1%	03888	PME55
R12	012043	RES	MF	249 OHM	T-9	.1%	03888	PME55
R13	000223	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R14	010536	RES	METAL	100 K		1% 1/10W	81349	RN55C1003F
R15	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R16	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R17	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R18	012044	RES	MF	499 K	T-9	.1%	03888	PME60
R19	040261	POT	CERMET	2 K		20% 1/2W	73138	72XW2K
R20	012045	RES	MF	54.9 K	T-9	.1%	03888	PME55
R21	040259	POT	CERMET	200 OHM		20% 1/2W	73138	72XW200
R22	012046	RES	MF	4.75 K	T-9	.1%	03888	PME55
R23	040256	POT	CERMET	20 OHM		20% 1/2W	73138	72XW20
R24	012047	RES	MF	210 OHM	T-9	.1%	03888	PME55
R25	012031	RES	METAL	FSV		1%	21793	012031
R26	010802	RES	METAL	FSV		1%	21793	010802
R27	010802	RES	METAL	FSV		1%	21793	010802
R28	012031	RES	METAL	FSV		1%	21793	012031
R29	010802	RES	METAL	FSV		1%	21793	010802
W1	600245	JUMPER	INSULATED					L-2007-1LP

RACAL-DANA Instruments Inc.

U. S. AND CANADIAN SERVICE CENTERS



FACTORY SERVICE LOCATIONS

(A) RACAL-DANA INSTRUMENTS INC.
18912 Von Karman Avenue
Irvine, California 92715
Telephone: (714) 833-1234

PRODUCT SERVICE TWX 910-595-1136

(B) RACAL-DANA INSTRUMENTS INC.
1400 Coleman, Suite G-27
Santa Clara, California 95050
Telephone (408) 727-2342

AUTHORIZED SERVICE CENTERS

(1) BALL AEROSPACE SYSTEMS DIVISION
P. O. Box 1062 - P. O. Box Zip 80306
Boulder Industrial Park
Boulder, Colorado 80302
Telephone: (303) 441-4786

(2) PAT JENKS ASSOCIATES
114 Cummings Park
Woburn, Massachusetts 01801
Telephone: (617) 938-0488

(3) RHODES-GROOS LABORATORIES
3409 Andtree Blvd.
Austin, Texas 78724
Telephone: (512) 928-0813

(4) WEBSTER INSTRUMENTS LTD.
1200 Aerowood Drive, Unit 28
Mississauga, Ontario
Canada L4W 2S7
Telephone: (416) 625-0600
TWX: 610-492-4560

RACAL-DANA Instruments Inc.

U. S. REPRESENTATIVES

ALABAMA

Saber Associates
P. O. Box 2311
Mobile, AL 36601
(800) 327-8998

ALASKA - See Oregon

ARIZONA

PLS Associates Inc.
4001 North 31st Ave.
Suite 61
Phoenix, AZ 85017
(602) 279-1531

ARKANSAS - See Oklahoma

CALIFORNIA

Northern:
Racal-Dana Instruments Inc.
Airport Park Office Bldg.
1400 Coleman Ave. Suite G-27
Santa Clara, CA 95050
(408) 727-2342

Southern:
Racal-Dana Instruments Inc.
18912 Von Karman Ave.
P.O. Box C-19541
Irvine, CA 92713
(714) 833-2780
(213) 628-8825

COLORADO

PLS Associates Inc.
7755 E. Quincy Ave. T-9
Denver, CO 80237
(303) 773-1218

CONNECTICUT - See Massachusetts

DELAWARE

Racal-Dana Instruments Inc.
(609) 853-1605
Also See Virginia
(Regional Office)

DISTRICT OF COLUMBIA See Virginia

FLORIDA

Saber Associates - Head Office
2051 N.W. 17th Lane
Pompano Beach, FL 33064
(305) 973-8804 or
(800) 327-8998
(800) 432-5618 (FL only)

P.O. Box 517
Rockledge, FL 32955

P.O. Box 100
Longwood, FL 32750

P.O. Box 1763
Bradenton, FL 33506

P.O. Box 9773
Riviera Beach, FL 33411

P. O. Box 3732
Idialantic, FL 32902

GEORGIA

Saber Associates
P.O. Box 2148
Acworth, GA 30101

HAWAII - See Oregon

IDAHO

North: See Oregon
South: See Colorado

ILLINOIS

Comtel
3535 W. Peterson Avenue
Chicago, IL 60659
(312) 539-4838

INDIANA

Comtel
1259 W. 86th Street
Indianapolis, IN 46260
(317) 253-1681

IOWA

Comtel
204 Collins Rd., N.E.
Cedar Rapids, Iowa 52402
(319) 377-9434

KANSAS

Comtel
5920 Nall, Suite 102
Shawnee Mission, KS 66202
(913) 722-1030

KENTUCKY

Eastern: See Ohio (Englewood)
Western: See Indiana

LOUISIANA - See Texas

MAINE - See Massachusetts

MARYLAND – See Virginia

MASSACHUSETTS

Racal-Dana Instruments Inc.
(617) 890-7195
Also See Virginia
(Regional Office)

MICHIGAN

Carter, McCormic & Peirce
23995 Freeway Park Drive
Farmington, MI 48024
(313) 477-7700

MINNESOTA

Comtel
5100 Edina Industrial Blvd.
Minneapolis, MN 55435
(612) 835-3060

MISSISSIPPI - See Alabama

MISSOURI

Comtel
10270 Page Blvd. Suite 113
St. Louis, MO 63132
(314) 428-5508

MONTANA - See Oregon

NEBRASKA - See Kansas

NEVADA - See California

NEW HAMPSHIRE - See Massachusetts

NEW JERSEY

Southern: See Delaware
Northern:
Racal-Dana Instruments Inc.
(201) 423-3039
Also See Virginia
(Regional Office)

NEW MEXICO

PLS Associates, Inc.
4300 H Silver Avenue, S.E.
Albuquerque. NM 87108
(505) 255-2330

NEW YORK

Southern: See New Jersey North
Northern:
NYC & Long Island
Racal-Dana Instruments Inc.
(516) 242-3454
Also See Virginia
(Regional Office)

NORTH CAROLINA - See South Carolina

NORTH DAKOTA - See Minnesota

OHIO

Carter, McCormic & Peirce
15 Rockridge Road
Englewood, OH 45322
(513) 836-0951

22650 Lorain Rd.
Fairview Park, Ohio 44126
(216) 779-5100

OKLAHOMA

Data Marketing Associates
6921 S. Canton Ave.
Tulsa, OK 74186
(818) 496-1457

OREGON

Racal-Dana Instruments Inc.
(503) 241-8624

PENNSYLVANIA

Eastern: See Delaware

Western:
Carter, McCormic & Peirce
409 Beatty Road
Monroeville, PA 15146
(412) 372-4415

PUERTO RICO - See Alabama

RHODE ISLAND - See Massachusetts

SOUTH CAROLINA

Saber Associates
P.O. Box 21563
Columbia, S.C. 29221

SOUTH DAKOTA - See Minnesota

TENNESSEE - See Alabama

TEXAS

Data Marketing Associates
3330 Bering Dr.
Houston, TX 77057
(713) 780-2511

14235 Proton Road
Dallas, TX 75234
(214) 661-0300

833 Isom Road
San Antonio, TX 78216
(512) 342-3031

300 Huntland Dr., Ste 233
Austin, TX 78752
(512) 451-5174

UTAH

PLS Associates, Inc.
2520 South State, Suite 152
Salt Lake City, Utah 84115
(801) 466-8729

VERMONT - See Massachusetts

VIRGINIA

P. O. Box 1326
Springfield, VA 22151
(703) 941-5983

WASHINGTON – See Oregon

WEST VIRGINIA

Eastern: See Virginia
Western: See Pa. (Western)

WISCONSIN

Comtel
21415 W. Greenfield Ave.
New Berlin, Wisc. 53151
(414) 544-6042

WYOMING - See Colorado

CANADA

Webster Instruments Ltd.
1200 Aerowood Drive Unit 28
Mississauga, Ontario
Canada L4W 2S7
(416) 625-0600

880 Lady Ellen Place Suite 3
Ottawa, Ontario
Canada K1Z569
(613) 725-1931

750 Laurentien Blvd. Suite 315
St. Laurent P. Q.
Canada H4M2M4
(514) 744-5829

#208 Campbell Centre
200 Carnegie Drive
St. Albert, Alberta
Canada T8N 3K1
(403) 458-4669

4211 Kingsway - Suite 509
Barnaby, B. C. V5H 3Y6
(604) 434-2611

REPAIR REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline and include a copy with your instrument to be sent to your local Racal-Dana repair facility.

Model Number _____ Options _____ Date _____

Serial Number _____ P. O.# _____

Company Name _____

Address _____

City _____ State _____ Zip Code _____

Contact _____ Phone Number _____

1. Describe, in detail, the problem and symptoms you are having.

_____

_____

2. If you are using your unit on the bus, please list the program strings used and the controller type, if possible.

_____

_____

3. List all input levels, and frequencies this failure occurs.

_____

_____

4. Indicate any repair work previously performed.

_____

_____

5. Please give any additional information you feel would be beneficial in facilitating a faster repair time. (I. E., modifications, etc.)

_____

_____